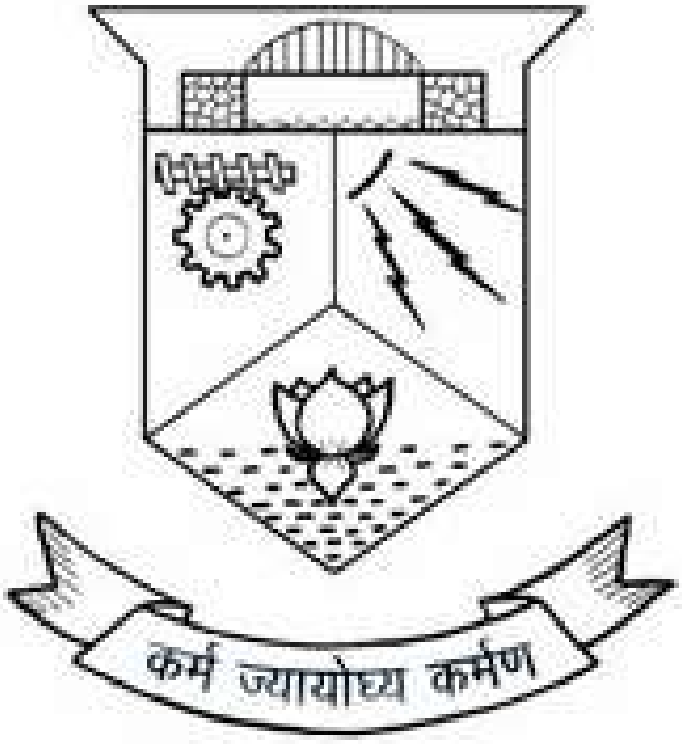
LABORATORY MANUAL

of

ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB – ECL 331



COLLEGE OF ENGINEERING, TRIVANDRUM

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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CERTIFICATE

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ECL 331	ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble :

This course aims to:

(i) Familiarize students with Analog Integrated Circuits and design and implementation of application circuits using basic Analog Integrated Circuits.

(ii) Familiarize students with simulation of basic Analog Integrated Circuits.

Course Outcomes: After the completion of the course, the student will be able to

CO No	Course Outcome Description
CO 1	Use data sheets of basic Analog Integrated Circuits and design and implement application circuits using Analog ICs.
CO 2	Design and simulate the application circuits with Analog Integrated Circuits using simulation tools.
CO 3	Function effectively as an individual and in a team to accomplish the given task.
CO 4	Analyze and troubleshoot the performance of basic analog circuits using appropriate testing equipment.

(ii) CO-PO/PSO matrix showing level of correlation (1-Low, 2-Medium, and 3-high)

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	3					2	2				3		
CO2	3	2			3			2	2	3				3	
CO3								2	3	3	2			3	
CO4	3	3		3	2			2	2	3					3

Assessment Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	3 hours

Continuous Evaluation Pattern

Attendance: 15 marks

Continuous Assessment: 30 marks

Internal Test (Immediately before the second series test): 30 marks

End Semester Examination Pattern

The following guidelines should be followed regarding award of marks:

(a) Preliminary work: 15 Marks

(b) Implementing the work/Conducting the experiment: 10 Marks

(c) Performance, result and inference (usage of equipments and troubleshooting): 25 Marks

(d) Viva voce: 20 Marks

(e) Record: 5 Marks

Cycle III: Simulation experiments using SPICE			
17	Difference Amplifier and Instrumentation amplifier	CO 2,3	68
18	Waveform generators using Op-Amps - Triangular and saw tooth	CO 2,3	71
19	Active second order filters using Op-Amp (LPF, HPF, BPF and BSF)	CO 2,3	74
20	A/D converters- counter ramp and flash type	CO 2,3	79

Cycle I : Analog Integrated Circuits Lab

EXPERIMENT NO. 1

Familiarization of Operational Amplifiers and Basic Circuits

Inverting and Non-Inverting Amplifiers, Frequency Response, Adder, Integrator

Aim

To familiarize with basic operational amplifier integrated circuits.

Components required:

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

Operational amplifier, in short, op-amp is a versatile device used to amplify AC and DC signals. Though it was originally designed for computing mathematical operations such as addition, multiplication, differentiation, integration etc., it is widely used for variety of applications like oscillators, filters, regulators, clipping circuits, waveform generators etc. The symbol of op-amp represents a circuit with two input terminals an output terminal and two bias supply points

The 741 IC: It is a frequency compensated and short circuit protected IC. The 741C is its commercial version, with operating temperature ranges from 0°C to +70°C. The 741 requires positive and negative dc sources for bias supply connections V+ and V-. This is provided by either a dual power supply or two power supplies. When dual power supply is used its positive terminal is connected to the V+ pin of the IC and the negative terminal is connected to the V- pin of the IC. The ground terminal of the dual power supply is connected to the ground point of the circuit. When two power supplies are used positive terminal of one supply and negative terminal of the other power supply are connected to the V+ and V- pins of the IC respectively. Inverting Amplifier: This is one of the most popular op-amp circuits. The polarity of the input voltage gets inverted at the output. If a sine wave is fed to the input of this amplifier, the output

will be an amplified sine wave with 1800 phase shift. The gain of the inverting amplifier is given by

A= -Rf/Ri. where Rf is the feedback resistance and Ri is the input resistance.

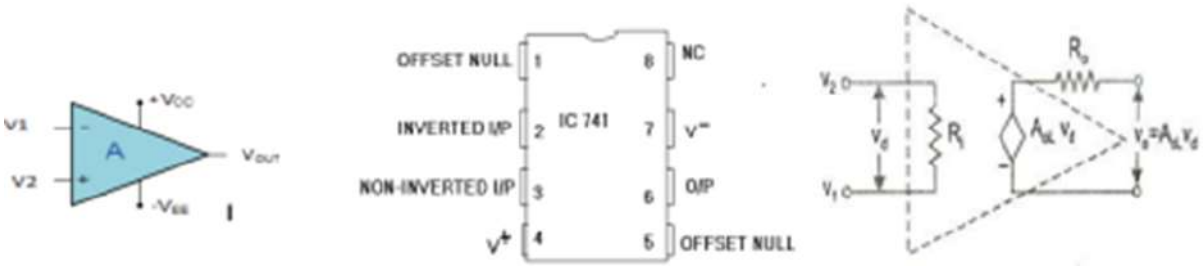
Non Inverting Amplifier: This circuit provides a gain to the input signal without any change in polarity. The gain of non-inverting amplifier is given by A=1+Rf/Ri. Input impedance is extremely large. Adder: This circuit gives the sum of two input voltages. Here an input voltage Vi and a dc voltage Vref are given as inputs to the adder. This is an inverting summing amplifier because the out is the sum of inputs with a sign change. The minus sign in the expression for the output can be avoided if necessary, by inverting the output once again using a unity gain inverting amplifier. The output can be scaled by selecting the ratio Rf/Ri. If this ratio is greater than 1 the circuit will function as a summing amplifier. Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by

$$V_o = -\frac{1}{R_1 C_f}\int_0^t V_i\, dt$$

At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor. Comparator: This circuit compares one analog voltage level with another analog voltage level or some preset reference voltage, VREF, and produces an output signal based on this voltage comparison. The op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two. The output saturation voltages are about 2V below the magnitudes of the dc power supply levels. For supply voltages of (+-15V),Vsat will be approximately (+-13V).

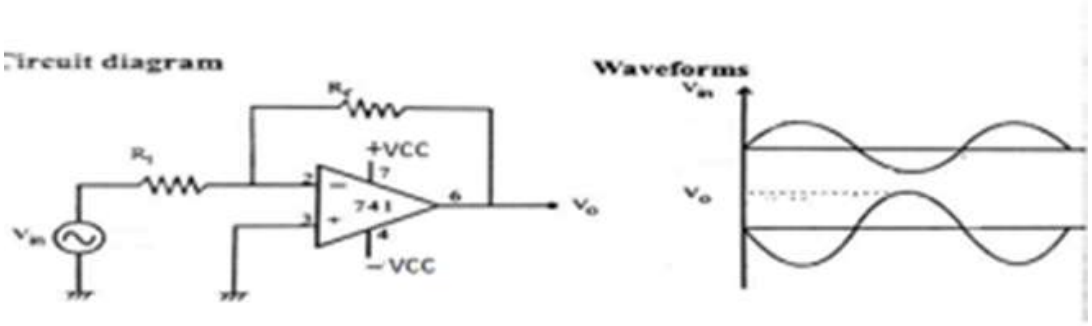
Sr. No.	Characteristics	Value for IC 741	Ideal value
1	Input resistance Ri	2 MΩ	∞
2	Output resistance Ro	75 Ω	0
3	Voltage gain Av	$2 X 10^5$	∞
4	Bandwidth BW	1 MHz	∞
5	CMRR	90 dB	∞
6	Slew rate S	0.5 V/μS	∞
7	Input offset voltage	2 mV	0
8	PSRR	150 μV/V	0
9	Input bias current	50 nA	0
10	Input offset current	6 nA	0

Circuit Diagram



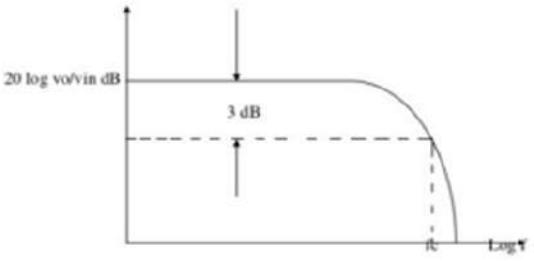
Op-amp symbol, Op-amp pinout, and equivalent circuit

Inverting amplifier



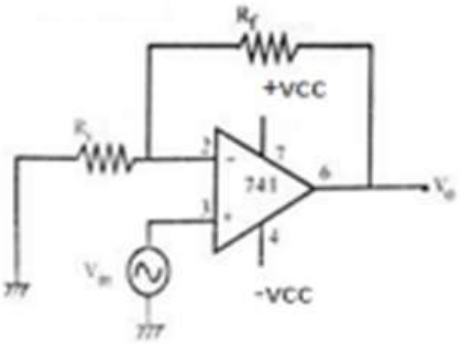
Tabular Column & Frequency Response

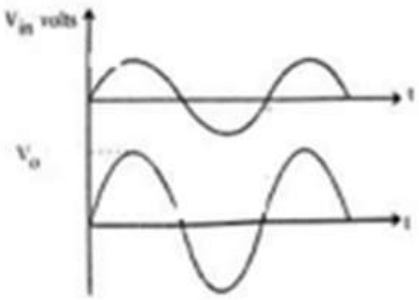
F(Hz)	V_0 (volts)	log f	$20\log(V_0/V_{in})$db



Non-Inverting Amplifier

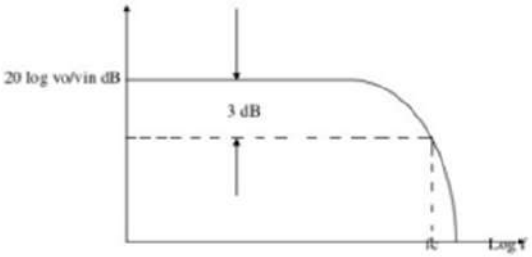
Circuit Diagram & Waveform





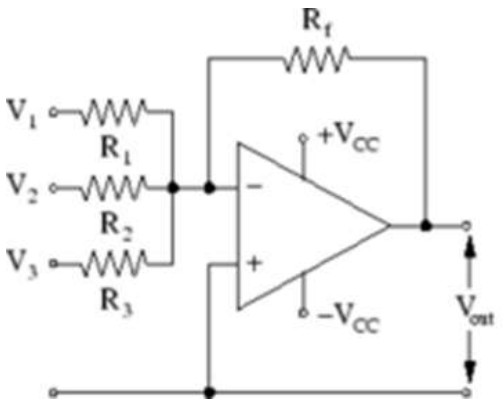
Tabular Column & Frequency Response

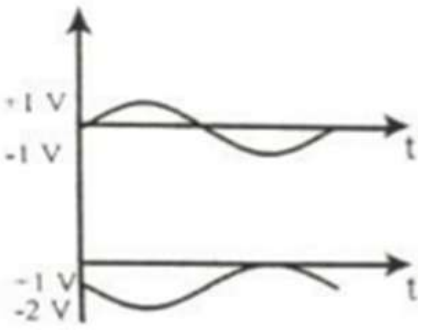
F(Hz)	V_0 (volts)	log f	$20\log(V_0/V_{in})$db



Adder

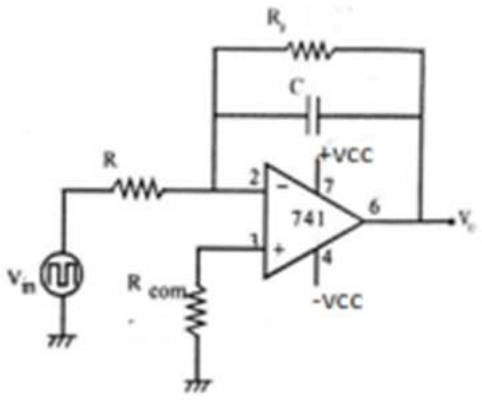
Circuit Diagram & Waveforms

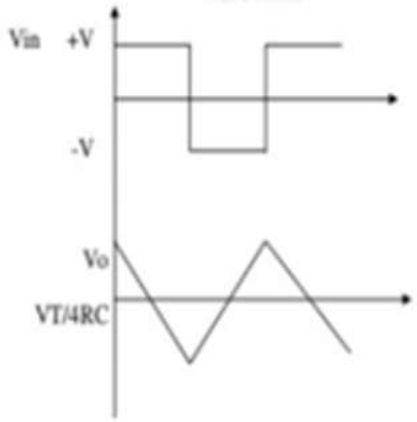




Integrator

Circuit Diagram & Waveforms

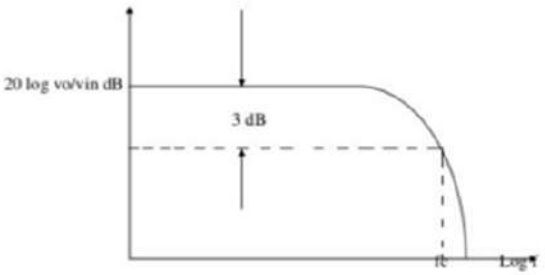


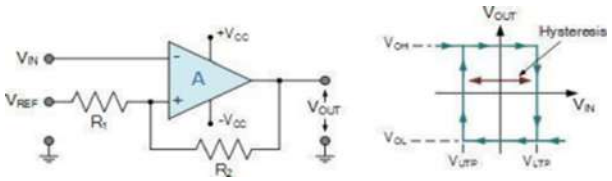


Tabular Column & Frequency Response

V_0 (volts)

F(Hz)	V_0 (volts)	log f	$20\log(V_0/V_{in})$db





Comparator

Circuit Diagram & Waveforms

Design

Inverting Amplifier

$$A = -\frac{R_f}{R_1}$$

Take $A = 1$

$$R_f = R_1$$

Choose $R_f = R_1$

Non-Inverting Amplifier

$$A = 1 + \frac{R_f}{R_1}$$

Take $A = 2$

$$R_f = R_1$$

Integrator

Let the input frequency be $f = 1$ kHz

$$f = \frac{1}{2\pi RC}$$

Take $C = 0.01$ μF and calculate R.

Select $R_f = 10\,R$

Procedure

I. Inverting Amplifier and Non-Inverting Amplifier

1. Set up the inverting amplifier on the breadboard.
2. Feed a 2 V_{pp} sine wave and observe the input and output simultaneously on the CRO. Verify whether the output is 22 V_{pp} sine wave in phase with the input.
3. Set up the non-inverting amplifier on the breadboard.
4. Feed a 2 V_{pp} sine wave and observe the input and output simultaneously on the CRO. Verify whether the output is 20 V_{pp} sine wave with 180° out of phase with the input.

II. Integrator

1. Set up the integrator circuit.
2. Feed a ..... , ... square wave at the input and observe the input and output simultaneously on the CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter the results in a tabular column and plot the frequency response.

III. Comparator

1. Set up the comparator circuit.
2. Feed the inputs and verify the output.

Results:

Familiarized with basic operational amplifier integrated circuits.

Gain of inverting amplifier :. . . . . .

Gain of non-inverting amplifier: :. . . . . .

EXPERIMENT NO. 2

Measurement of Op-Amp parameters

Aim

To measure the following parameters of an Op-amp i.e, input bias current, input offset voltage, input offset current, CMRR and slew rate.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

Op-Amp Parameters

Input bias current IB: It is defined as the average of the currents entering into the inverting and non-inverting terminals of an op-amp.

$I_B = \frac{I_{b1}+I_{b2}}{2}$

Typical value of input bias current is 80nA.

Input offset current IOs: It is defined as the algebraic difference between the currents entering into the inverting and non-inverting terminals of an op-amp.

$$IO = |Ib1 - Ib2|$$

Typical value of input offset current is 20nA.

Input offset voltage: It is defined as the small voltage which is applied to overcome circuit imbalances due to which the output voltage is not zero for zero input voltage, ie voltage applied between the input terminals of an op-amp to nullify the output voltage. Typical value of input offset voltage is 2mV.

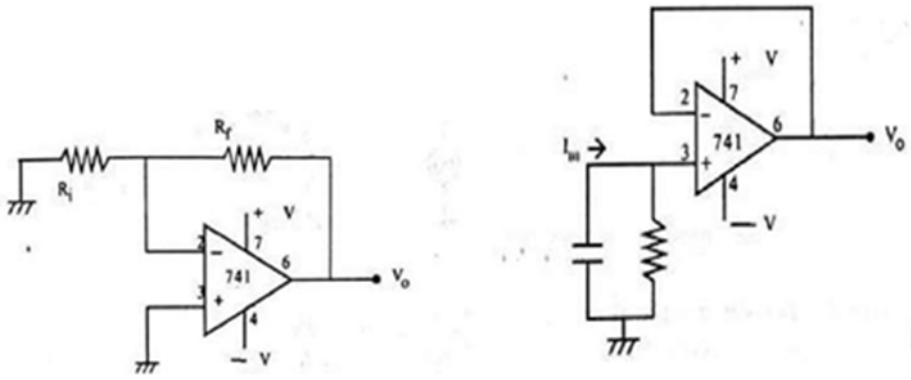
CMRR: It is the ratio of differential mode gain to common mode gain and is expressed in dB.

$$CMRR = 20\log(Ad/Ac) \text{ in dB}$$

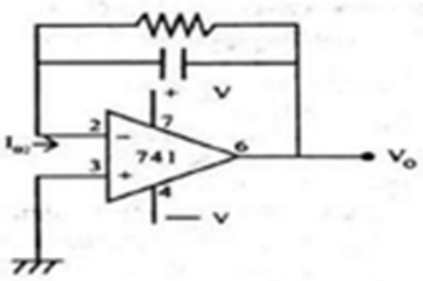
Slew rate: It is the rate of rise of output voltage. It is a measure of the speed of op-amp. It is expressed in v/μs.

Circuit diagrams:

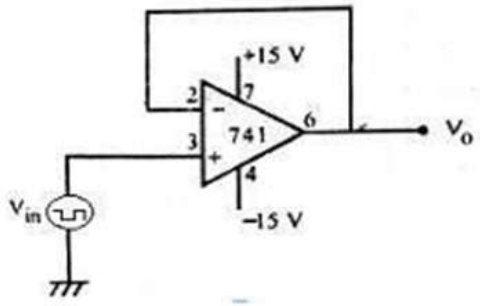
Circuit to measure input offset voltage



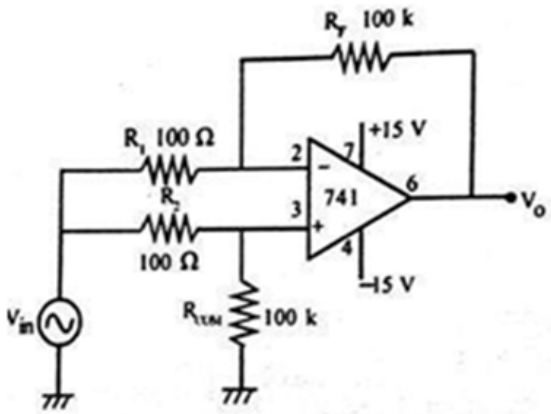
Circuit to measure IB1



Circuit to measure slew rate



Circuit to measure CMRR



Procedure

1. Set up the circuit to find the input offset voltage.
2. Measure the output voltage using the expression,

$$ViO = \frac{VO\ Ri}{Rf + Ri}$$

   where Vo is the output voltage and Vio is the input offset voltage.

3. Set up the circuits for measuring input bias current and input bias voltage.
4. Measure the output voltage using the expressions

$$Vo = Ib1\ R \quad \text{and} \quad Vo = Ib2\ R$$

5. Calculate $IB1$ and $IB2$ and measure the bias and offset currents using the expressions

$$IB = \frac{Ib1 + Ib2}{2} \quad \text{and} \quad IOS = |Ib1 - Ib2|$$

   where IB is bias current and IO is offset current.

6. Set up the circuit to calculate the slew rate. Give a square input of . . . ., ... Vary the input frequency and observe the output. Note down the frequency at which the output gets disturbed. Calculate the slew rate using the expression

$$SR = \frac{2\pi f V_m}{10^6}$$

7. Set up the circuits for finding CMRR and apply a dc signal of . . . V to input and measure VO. Calculate the CMRR using the expression

$$CMRR = \frac{Vi(Rf/Ri)}{VO}$$

   Express the CMRR in dB using the expression

$$20\log(CMRR)$$

Results

Measured the Op-amp parameters and obtain the following:

- Input offset voltage = ... mV
- Input bias current = ... A
- Input offset current = ... A
- Slew rate = ... V/µs
- CMRR = ...

EXPERIMENT NO. 3

Schmitt trigger circuit using op amps

Aim

To design and set up a Schmitt trigger circuit using op-amps for various LTP and UTP.

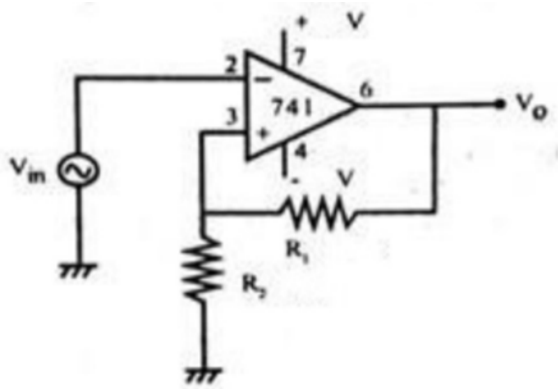
Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

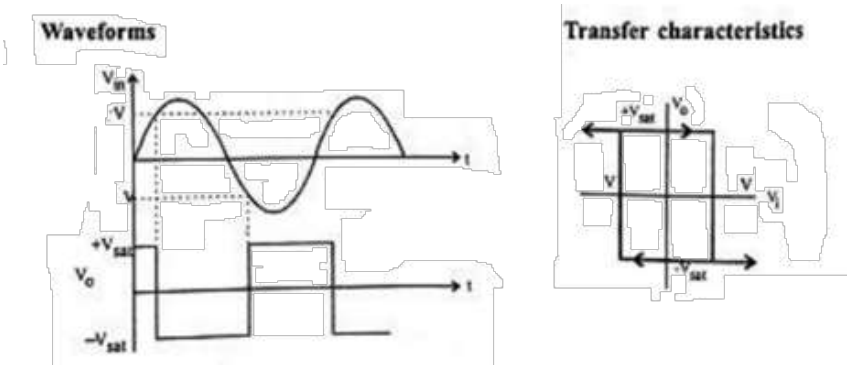
Theory

Schmitt Trigger converts an irregular shaped waveform to a square wave or pulse. Here, the input voltage triggers the output voltage every time it exceeds certain voltage levels called the upper threshold voltage V_{UTP} and lower threshold voltage V_{LTP}. The input voltage is applied to the inverting input. Because the feedback voltage is aiding the input voltage, the feedback is positive. A comparator using positive feedback is usually called a Schmitt Trigger. Schmitt Trigger is used as a squaring circuit, in digital circuitry, amplitude comparator, etc.

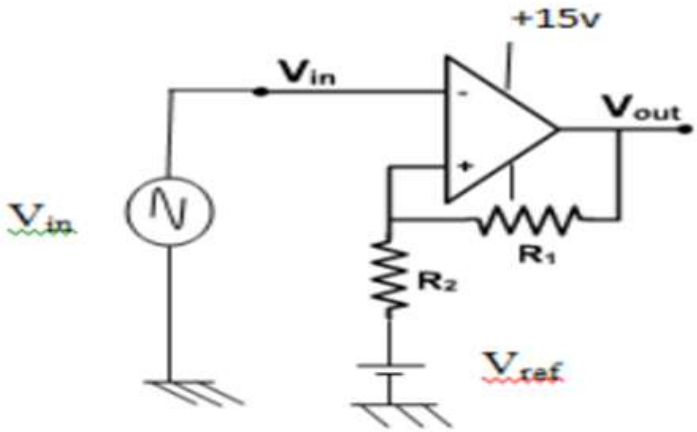
Circuit diagram

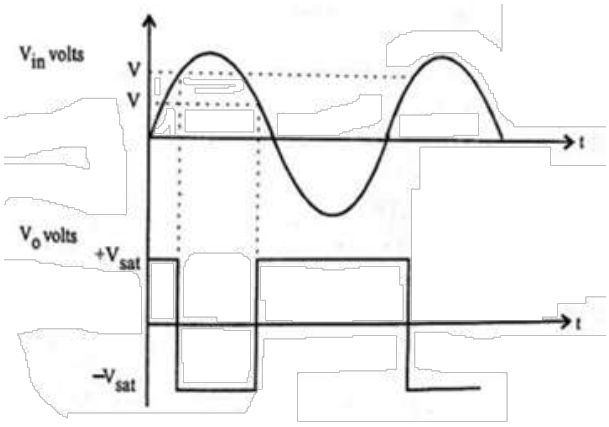


Schmitt trigger LTP=.....V and UTP=.....V



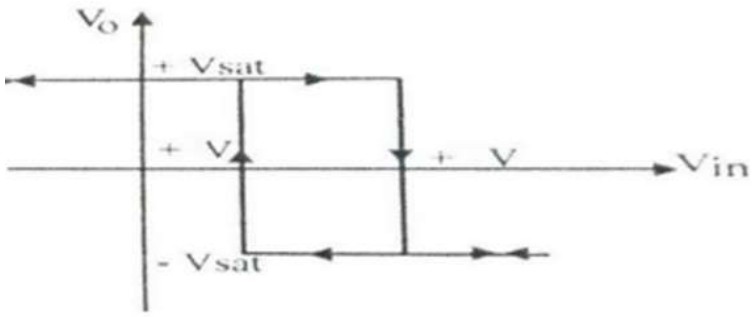
Schmitt trigger LTP=.....V and UTP=.....V



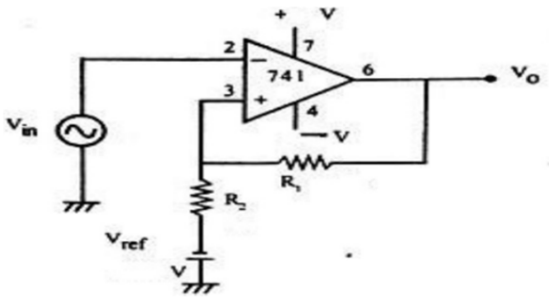


Waveform

Transfer Characteristics



Schmitt trigger LTP=.....V and UTP=.....V



Design :

Schmitt trigger LTP = ... V and UTP = ... V

Let the required LTP be . . . .V and UTP be V

Assume, V_{sat} = ... V when V^+ = ...V as reference voltage.

$$LTP = ... = \frac{-13R_2}{R_1 + R_2} + \frac{V_{ref}R_1}{R_1 + R_2}$$

$$UTP = ... = \frac{13R_2}{R_1 + R_2} + \frac{V_{ref}R_1}{R_1 + R_2}$$

Take R_2 = ... K and R_1 = ... K

Schmitt trigger LTP = ... V and UTP = ... V

Let the required LTP be . . . .V and UTP be V

Assume, V_{sat} = ... V when V^+ = ...V as reference voltage.

$$LTP = ... = \frac{-13R_2}{R_1 + R_2} + \frac{V_{ref}R_1}{R_1 + R_2}$$

$$UTP = ... = \frac{13R_2}{R_1 + R_2} + \frac{V_{ref}R_1}{R_1 + R_2}$$

Take $R_2 = ...$ K and $R_1 = ...$ K

We get reference voltage $V_{ref} = ...$ V

Schmitt trigger $LTP = ...$ V and $UTP = ...$ V

Let the required LTP be ....V and UTP be V

Assume, $V_{sat} = ...$ V when $V^+ = ...$V as reference voltage.

$$LTP = ... = \frac{-13R_2}{R_1 + R_2} + \frac{V_{ref}R_1}{R_1 + R_2}$$

$$UTP = ... = \frac{13R_2}{R_1 + R_2} + \frac{V_{ref}R_1}{R_1 + R_2}$$

Take $R_2 = ...$ K and $R_1 = ...$ K

We get reference voltage $V_{ref} = ...$ V

Procedure

1. Verify whether the op-amp was in good condition.
2. Set up the circuit for Schmitt trigger and switch on the supplies and observe the input and output on the CRO screen.
3. Observe the transfer characteristics.

Results

Designed the Schmitt trigger and obtained the output

EXPERIMENT NO. 4

Difference Amplifier And Instrumentation Amplifier

Aim

To design and setup a difference amplifier and instrumentation amplifier using op amp.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator power supplies.

Theory

The difference amplifier circuit is very useful in detecting very small differences in the signal. Since the gain is R_F/R_1, it can be selected to be very large. The output

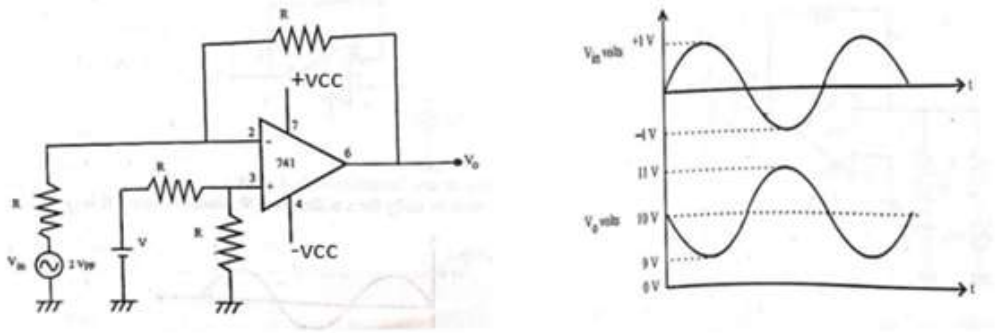
$$V_O = -\frac{R_F}{R_1}(V_2 - V_1)$$

If all the external resistors are of equal value, the gain of the amplifier becomes one. Thus the output is $V_2 - V_1$. Hence the name subtractor.

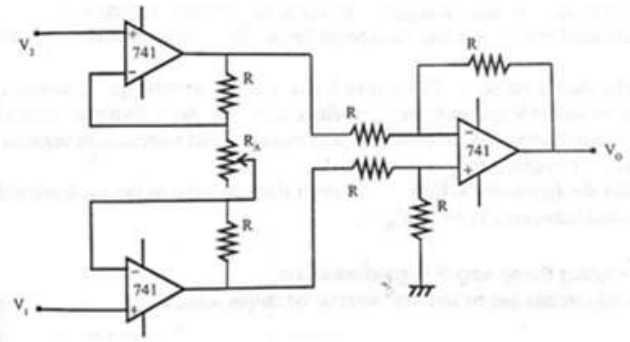
Instrumentation amplifiers are widely used in data acquisition systems, remote sensing applications, and instrumentation systems to measure temperature, humidity, light intensity, and weight, etc. Most of the instrumentation systems use a transducer in a bridge circuit. Instrumentation amplifier facilitates the amplification of potential difference that takes place due to the imbalance of the bridge circuit proportional to a change in physical quantity. The main features of instrumentation amplifiers are high gain, high input resistance, high CMRR, etc.

Circuit diagram and waveforms:

Difference amplifier



Instrumentation amplifier



Design :

Difference amplifier:

$$V_0 = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) - V_2\left(\frac{R}{R}\right) = V_1 - V_2$$

Instrumentation amplifier :

We have,

$$V_0 = (V_1 - V_2)\left[1 + \frac{2R}{R_A}\right]$$

Given,

$$1 + \frac{2R}{R_A} = 3$$

Assume R and RA 10K. Use 10K pot in series with 470Ω

Procedure

1. Verify the condition of op-amps.
2. Setup the circuit.
3. Verify the output.

Results

Designed the difference and instrumentation amplifier.

EXPERIMENT NO. 5

Waveform generators using Op-Amps - Triangular and Saw tooth

Aim

To set up and study a saw-tooth and triangular wave form generator using Op-Amp for 1KHz frequency.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

Triangular wave generator:

This circuit uses two op-amps. One functions as a comparator and the other as an integrator. The comparator compares the voltage at point P continuously with respect to the point voltage at the inverting input, which is at zero volt. When voltage at P goes slightly above zero, the output of A1 switches to negative saturation. Suppose the output of A1 is at positive saturation $+V_{\text{sat}}$; since this voltage is at the input of the integrator, the output of A2 will be a negative-going ramp. Thus, one end of the voltage divider R_1 and R_2 is at $+V_{\text{sat}}$ and the other end is at the negative-going ramp.

At the time $t = t_1$, when the negative-going ramp attains the value of $-V_{\text{ramp}}$, the effective voltage at P becomes slightly less than zero volt. This switches the output of A1 from $+V_{\text{sat}}$ to $-V_{\text{sat}}$ level. The output of A2 increases in the positive direction. At the instant $t = t_2$, the voltage at P becomes just above zero volt, thereby switching the output of A1 from $-V_{\text{sat}}$ to $+V_{\text{sat}}$. The cycle repeats and generates a triangular waveform.

Frequency of the triangular waveform:

$$f = \frac{R_1}{4R_2R_3C}$$

Peak-to-peak amplitude of ramp voltage:

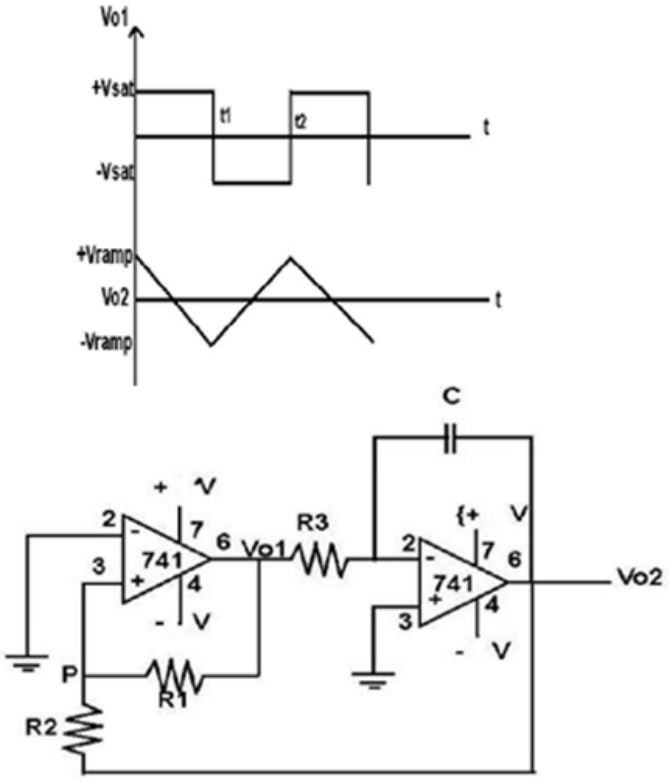
$$V_{pp} = 2\frac{R_2}{R_1}V_{sat}$$

Saw tooth waveform generator:

In a sawtooth waveform generator, the rise time is much higher than its fall time or vice-versa. The triangular waveform generator can be converted into a sawtooth waveform generator by including a variable DC voltage into the non-inverting terminal of the integrator. This can be done by using a potentiometer. When the wiper of the potentiometer is at the centre, the output will be a triangular wave since the duty cycle is 50%. If the wiper moves towards the negative, the rise time of the sawtooth becomes larger than the fall time. If the wiper moves towards the positive, the fall time becomes larger than the rise time. The sawtooth waveform generators have wide applications in time-base generators and pulse-width modulation circuits.

Circuit diagram and waveforms:

Triangular wave generator



Design :

Triangular wave generator:

Frequency, $f = \frac{R_1}{4R_2R_3C}$

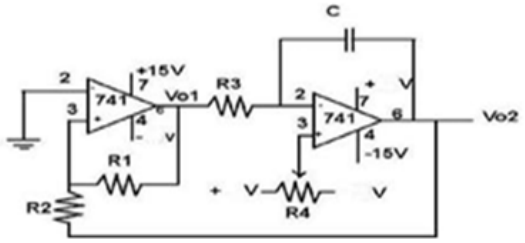
Peak-to-peak output of ramp $V_{pp} = \frac{2R_2}{R_1}V_{sat}$

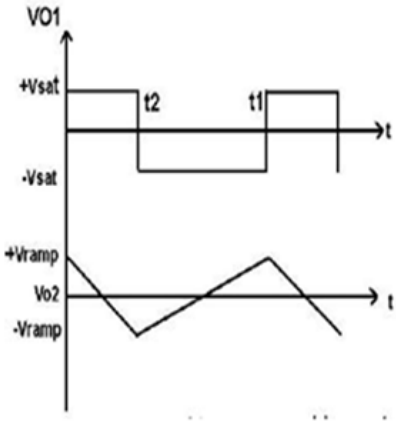
Let the required $V_{pp} = \ldots$ V and $V_{sat} = \ldots$ V.

Assume $R_1 = \ldots$ kΩ then $R_2 = \ldots$ Ω.

Take $C = \ldots$ μF, so $R_3 = \ldots$ kΩ.

Sawtooth wave generator





Design :

Sawtooth wave generator:

Frequency, $f = \frac{R_1}{4R_2R_3C}$

Peak-to-peak output of ramp $V_{pp} = \frac{2R_2}{R_1}V_{sat}$

Let the required $V_{pp} = \ldots$ V and $V_{sat} = \ldots$ V.

Assume $R_1 = \ldots$ kΩ, then $R_2 = \ldots$ Ω (use $\ldots$ Ω standard).

Take $C = \ldots$ μF, so $R_3 = \ldots$ kΩ (use $\ldots$ kΩ pot).

Select $R_4 = \ldots$ kΩ.

Procedure

1. Set up the waveform generator circuit.
2. Obtain the output and note down the amplitude and frequency.
3. Set up the circuit of sawtooth wave generator.
4. Observe the output of both op-amps and note down the rise time and fall time.
5. Obtain the output by moving the wiper of port in both directions and observe the changes taking place in waveforms.

Results

Designed and studied the saw tooth and triangular wave generator.30

EXPERIMENT NO. 6

RC PHASE SHIFT OSCILLATOR

Aim

To design and set up an RC phase shift oscillator using op-amp for a frequency of 1 kHz.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies

Theory

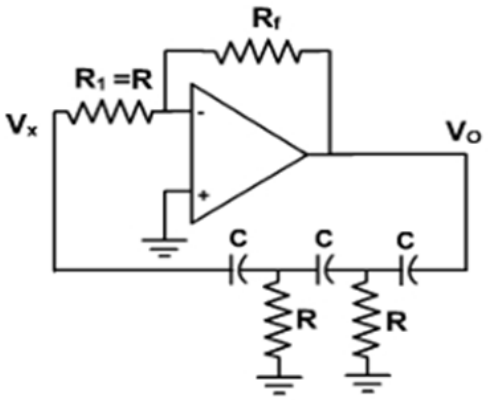
RC phase shift oscillator consists of an op-amp as the amplifying stage and three RC cascaded networks as the feedback network. The feedback network provides a fraction of the output voltage back to the input of the amplifier. The op-amp is functioning in the inverting mode. Therefore, any signal which appears at the inverting terminal is shifted by 180° at the output. An additional 180° phase shift required for oscillations per Barkhausen criteria, is provided by the cascaded RC network. Thus, the total phase shift around the loop becomes 0°.

The frequency of oscillation is given by,

$$f_o = \frac{1}{2\pi\sqrt{6}RC}$$

The gain of the inverting op-amp should be atleast 29 at this frequency because the attenuation provided by the feedback network is 1/29. The gain is kept slightly greater than 29 to ensure that the variations in circuit parameters will not make the loop gain less than unity, and thus oscillations died out. For lower frequencies (<1 MHz), op-amp 741 may be used, however for higher frequencies, LM318 or LF351 should be used.

Circuit diagram



Design

Let the required frequency be $f_0 = \frac{1}{2\pi\sqrt{RC}} \approx \ldots$ kHz.

Take $C = \ldots$ μF, then $R = \ldots$ Ω. Use $R = \ldots$ Ω.

Gain: Gain $= \frac{R_f}{R_1} = \ldots$.

Take $R_1 = \ldots$ kΩ, $R_f = \ldots$ kΩ (pot.).

Procedure

1. Verify whether the op-amp is in good condition and set up the circuit as shown in the circuit diagram.

2. Note down the amplitude and frequency of output waveform.

Results

Designed the RC phase shift oscillator using Op-amp.

EXPERIMENT NO. 7

Active second order filters using Op-Amp (LPF, HPF, BPF and BSF)

Aim

To design and set up the active second order filters using Op-amp.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

A stop band having a 40 dB/decade roll off is obtained with the second order filters. They are important because higher order filters can be realized using them. The gain of the second order filters can be fixed by R_1 & R_F, while the cutoff frequency can be obtained from R_2, R_3, C_2, and C_3 as

$$f = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

and voltage gain

$$A_V = 20\log\left(\frac{V_0}{V_{in}}\right).$$

For a second order low pass filter, the voltage gain magnitude is

$$\left|\frac{V_0}{V_i}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}}$$

For a second order high pass filter, the voltage gain magnitude is

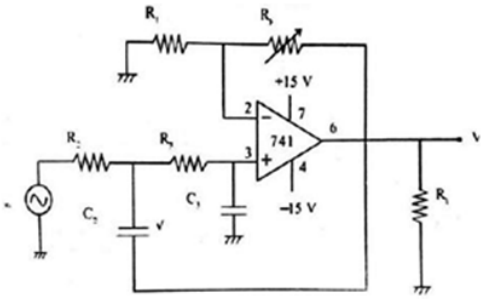
$$\left|\frac{V_0}{V_i}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f_L}{f}\right)^4}}$$

For a second order band pass filter, the voltage gain magnitude is

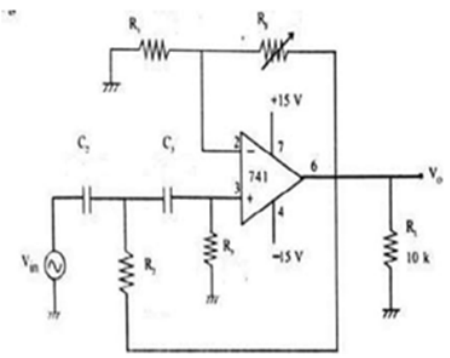
$$\left|\frac{V_0}{V_i}\right| = \frac{A_F\,(f/f_L)}{\sqrt{\left[1+\left(\frac{f}{f_L}\right)^2\right]\left[1+\left(\frac{f}{f_H}\right)^2\right]}}.$$

A band pass filter of -40 dB/decade fall off rate can be formed by cascading a second order HPF and LPF. A band reject filter is obtained by cascading a LPF, HPF and a summer circuit.

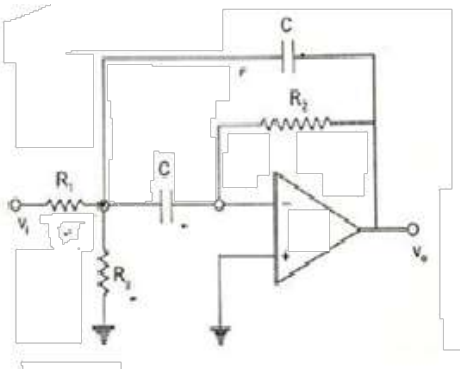
Circuit diagram and waveforms:



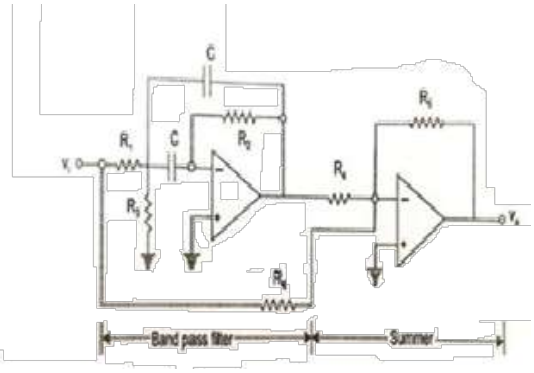
Low pass filter



High pass filter



Band pass filter



Band reject filter

Design :

Low pass filter design

Required cutoff frequency fH = . . . KHz.

We have $f_H = \dfrac{1}{2\pi\sqrt{R_1 R_2 C_2 C_3}}$.

Let $C_2 = C_3 = \ldots\ \mu$F. Then $R_2 = R_3 = \ldots$ K.

For $R_2 = R_3$ and $C_2 = C_3$,

The pass band gain $A_F = (1 + R_F/R_1)$ must be ….

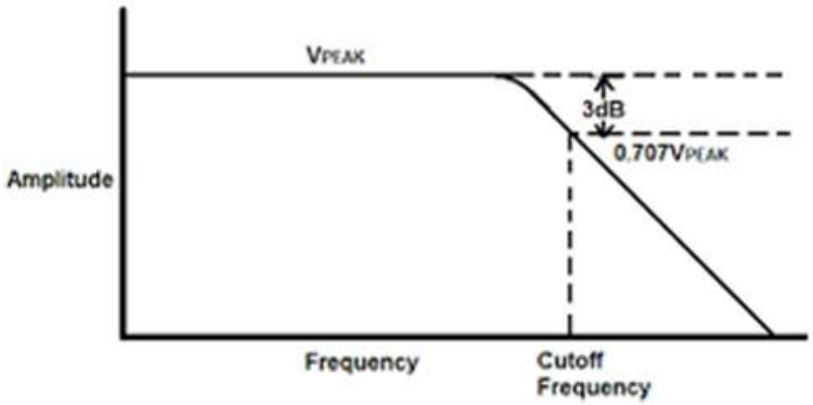
That is $R_F = \ldots R_1$.

Let $R_1 = \ldots$ K. Then $R_F = \ldots$ K (use … k).

Tabular Column Vin = …. volt

f(Hz)	V_0(V)	Log(f)	A_v in dB

Graph



High pass filter design

Given cutoff frequency $f_L = \ldots$ KHz. We have,

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Take $C_2 = C_3 = C$ and $R_2 = R_3 = R$.

Then $f_L = \dfrac{1}{2\pi RC}$.

Assume $C = \ldots\ \mu$F. Then $R = \ldots$ K. Use $\ldots$ k std.

The pass band gain $A_F = (1 + R_F/R_1)$ must be $\ldots$ for Butterworth filter.

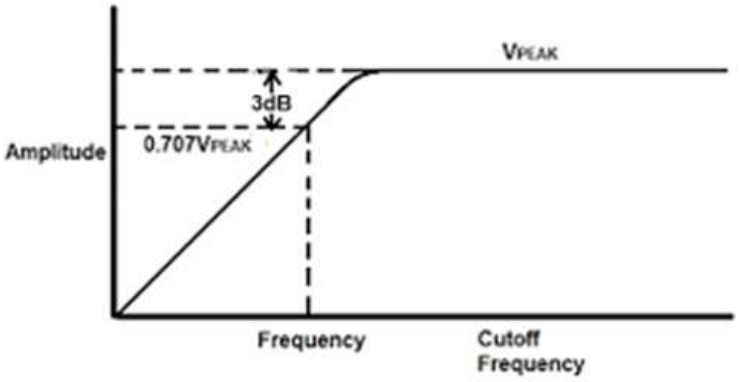
i.e. $R_F = \ldots R_1$.

Take $R_1 = \ldots$ K. Then $R_F = \ldots$ K. Use $\ldots$ K pot.

Tabular Column Vin = ... volt

f(Hz)	V_0(V)	Log(f)	A_v in dB

Graph

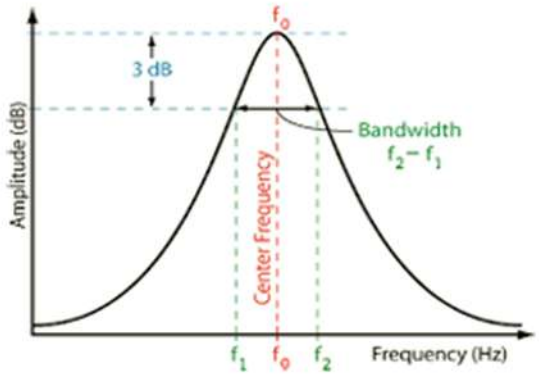


Band pass filter

Tabular Column Vin = ...volt

f(Hz)	V_0(V)	Log(f)	A_v in dB

Graph

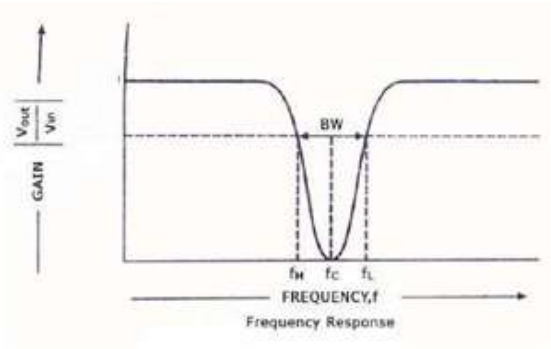


Band reject filter

Tabular Column Vin = ...volt

f(Hz)	V_0(V)	Log(f)	A_v in dB

Graph



Procedure

1. Set up the circuits and feed a . . . .Vpp sine wave from the signal generator.
2. Vary the frequency in steps and note the output voltage.
3. Plot the frequency response.
4. Mark the lower cut-off frequency and calculate the roll-off in dB/decade

Results

Designed the second order filters using op amp and obtained the results as Cutoff frequency of low pass filter =.....KHz

Roll off of low pass filter =. . . . . .

Cutoff frequency of high pass filter =.....KHz

Roll off of high pass filter =. . . . . .

Cutoff frequency of band pass filter =.....KHz

Roll off of band pass filter =. . . . . .

Cutoff frequency of band reject filter =.....KHz

Roll off of band reject filter =. . . . . .

EXPERIMENT NO. 8

Astable and Monostable multivibrator using Op –Amps

Aim

To design set up an astable and monostable multivibrators using op-amps for a frequency of 1kHz.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

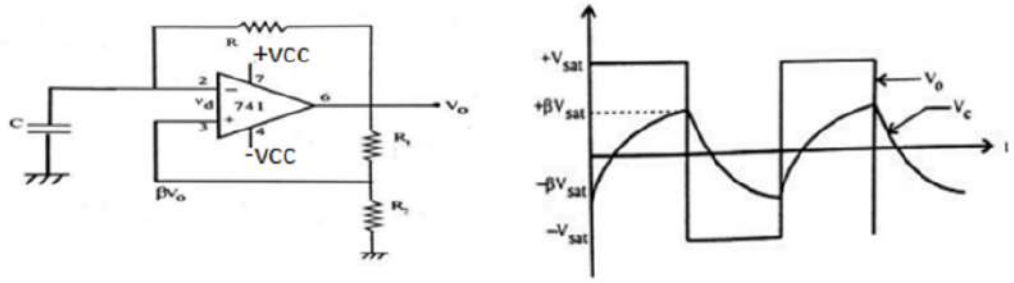
Astable multivibrator: Astable multivibrators are capable of producing square wave for given frequency, amplitude and duty cycle. The output of an op-amp is forced to swing repetitively between positive saturation $+V_{sat}$ and negative saturation $-V_{sat}$ resulting in a square wave output. This circuit is also called free running multivibrator or square wave generator. The output of the op-amp will be in positive saturation if differential input voltage is negative and vice versa. The differential voltage $V_d = V_c - \beta V_{sat}$ where β is the feedback factor. βV_{sat} is the potential at non-inverting terminal of op-amp. Consider the instant at which $V_o = +V_{sat}$. Now the capacitor charges exponentially towards $+V_{sat}$ through R. Automatically V_d increases and crosses zero. This happens when V_c changes to $-V_{sat}$. Now capacitor starts to discharge to zero and recharge towards $-V_{sat}$. Now V_d decreases and crosses zero. This happens when $V_c = -\beta V_{sat}$. The moment V_d becomes negative again, output changes to $+V_{sat}$. This completes one cycle. The time period T of the square wave is $T = 2RC \ln \frac{1+\beta}{1-\beta}$. If β is made 1/2, $T = 2.2RC$. Astable multivibrator is particularly useful for the generation of frequency in the audio frequency range. Higher frequencies are limited by the delay time and slew rate of the op-amp.

Monostable multivibrator: A Monostable Multivibrator, often called a one-shot Multivibrator, has a stable state and a quasi-stable state. The circuit remains in stable state until

triggering signal causes a transition to quasi-stable state. After a time interval, it returns to the stable state. So a single pulse of predetermined duration can be generated using this circuit. Consider the instant at which the output $V_o = +V_{sat}$. Now the diode D_1 clamps the capacitor voltage V_c at 0.7 V. Feedback voltage available at non-inverting terminal is $+\beta V_{sat}$. When the negative going trigger is applied such that potential at non-inverting terminal becomes less than 0.7 V, the output switches to $-V_{sat}$. Now the capacitor charges through R towards $-V_{sat}$, because the diode becomes reverse biased. When the capacitor voltage becomes more negative than $-V_{sat}$, the comparator switches back to $+V_{sat}$, and the capacitor C starts charging to $+V_{sat}$ through R until V_c reaches 0.7 V.

Circuit diagrams and waveforms:

Astable multivibrator



Design :

Required period of oscillation $T = \ldots$ ms with duty cycle 50%

Time period $T = T_1 + T_2 = 2RC \ln \frac{1+\beta}{1-\beta}$

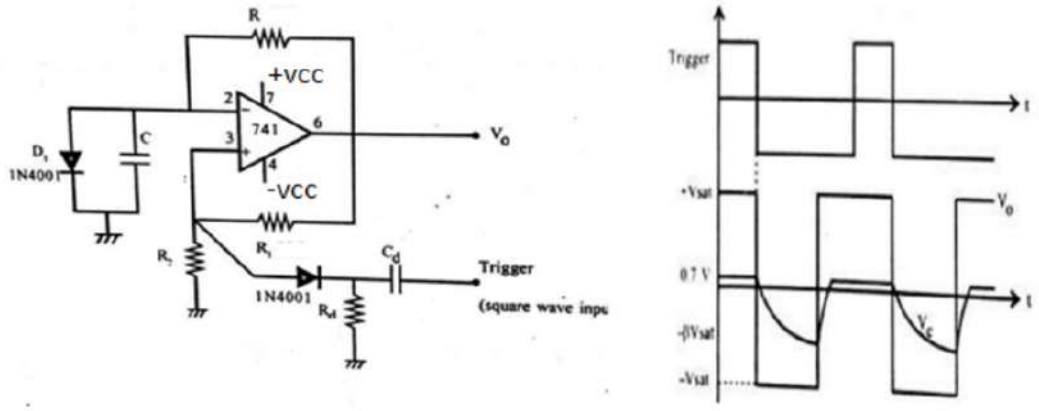
Where β, the feedback factor, $\beta = \frac{R_2}{R_1+R_2}$

Take $\beta = \ldots$ and $R_2 = 10$ K. Then

$R_1 = \ldots$ K. When $\beta = \ldots, T = \ldots RC$

Let C be $\ldots$ μF. Then $R = \ldots$ K.

Astable multivibrator



Design :

Required period of oscillation $T = \ldots$ ms with duty cycle 50%

Time period $T = RC \ln\left[\frac{1}{1-\beta}\right]$, $\quad T = \ldots RC$

Take $\beta = \ldots$ and $R_2 = \ldots$ K. Then $R_1 = \ldots$ K

Use $\ldots$ K

Design of differentiating circuit: $R_d C_d < 0.016 T_t$

Take trigger time period $T_t = \ldots$ ms and $C_d = \ldots$ 1 μF. Then $R_d = \ldots$ K

Procedure

1. Verify the conditions of op-amp.
2. Set up the circuit astable multivibrator and observe the output waveform. Note down their frequencies and amplitudes.
3. Set up the circuit monostable multivibrator and feed $\ldots$ V_{pp}, $\ldots$ Hz square wave at the trigger input and observe the output waveform. Note down their frequencies and amplitudes.

Results

Designed the astable and monostable multivibrator using Op-amp.

EXPERIMENT NO. 9

Precision rectifiers using Op-Amp.

Aim

To design and setup a precision rectifier using op amp

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

The precision rectifier, also known as a super diode, is a configuration obtained with an operational amplifier in order to have a circuit behave like an ideal diode and rectifier. It is useful for high-precision signal processing.

In a precision half wave rectifier, a diode is placed in the negative feedback path of the op amp. If V_{in} becomes positive, the output of the op amp will become positive. Hence the diode conducts and a closed feedback path is established between the op amp's output terminal and the negative input terminal. This negative feedback path will cause a virtual short circuit to appear between two input terminals. Thus $V_0 = V_{in}$. For the circuit to start working V_{in} has to exceed the voltage equal to diode drop/op amp open loop gain. Since the op amp open loop voltage is very high, starting voltage is negligibly small. Hence the circuit behaves like an ideal diode.

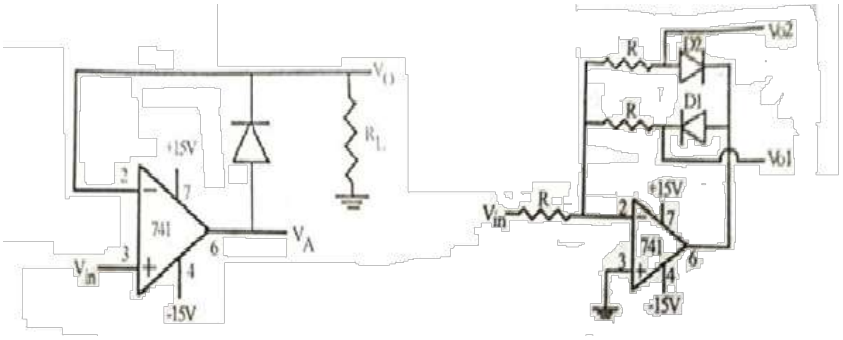
If V_{in} becomes negative, the output V_o of the op amp will be negative. This will reverse bias the diode and no current will flow through the load resistance R_L, causing the output V_O to remain at 0V. Since the diode is off, the op amp will be operating as open loop circuit and its output will be at $-V_{sat}$.

In a practical half wave precision rectifier an inverting amplifier is converted to a rectifier by adding two diodes. The resistors are designed such that gain of the amplifier is one. During the positive half cycle of the input, the output becomes negative. At this moment D_2 becomes

forward biased and D_1 becomes reverse biased. Hence V_{01} is zero and V_{02} is negative. During the negative half cycle, the output of the inverting amplifier becomes positive and D_1 becomes forward biased and D_2 becomes reverse biased. Hence the V_{01} is positive and V_{02} is zero.

A full wave precision rectifier consists of a half wave rectifier and an inverting adder. We can vary the output gain by changing the values of resistors as required. Input signal is directly given to the adder at X. The output V_{02} which gives the negative ripples only of the half wave rectifier is also given to the adder at Y. The mathematical addition of these two signals will give the output of a full wave rectifier. The resistance value of the adder is adjusted such that the output is $-(2Y + X)$.

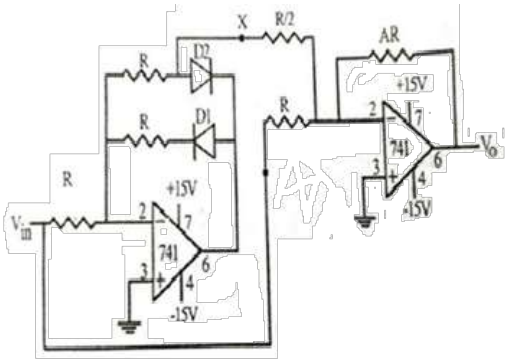
Circuit diagram and waveforms:

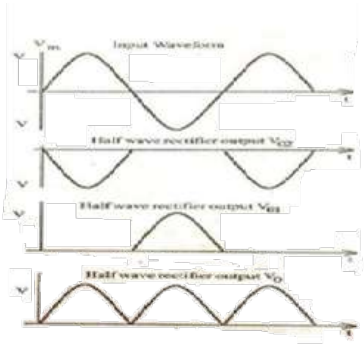


Half wave precision rectifier

Practical half wave precision rectifier

Full wave precision rectifier





Design :

For unity gain select R=. . . ..K

Procedure

1. Set up the circuit.
2. Apply a sine wave of milli-volt range and frequency less than . . . ..KHz.
3. Observe the output in the CRO.
4. Repeat the procedure for the full wave circuit.

Results

Designed the circuit for precision rectifier and obtained the result.

EXPERIMENT NO. 10

WIENBRIDGE OSCILLATOR USING OP-AMP WITH AND WITHOUT AMPLITUDE STABILIZATION

Aim

1. To design set up a wien bridge oscillator incorporating amplitude stabilization
2. Design and set up a Wien bridge oscillator using an op-amp for a frequency of 1kHz.

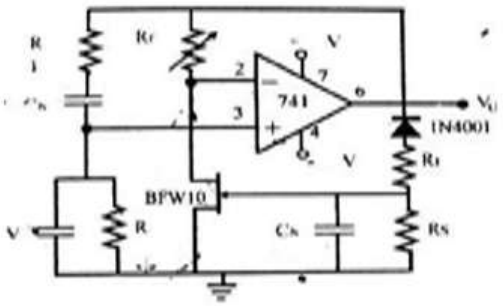
Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies

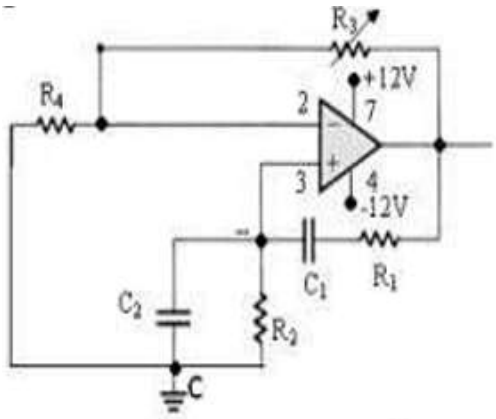
Theory

An FET circuit in association with the wien bridge oscillator, helps the stabilization of the amplitude of oscillation. The N-channel JFET acts as a voltage controlled resistor and the diode circuit function as a negative peak detector. The dc voltage at the gate of FET becomes more negative when amplitude of oscillation increases. Then gate of FET gets reverse biased and effective resistance from drain to source increases. This causes to decrease the gain according to the relation $A = 1 + (R_f/R_i)$ and amplitude is brought back to a stable level. When output peak starts to decrease, opposite patter occurs. This is an audio frequency oscillator of high stability and simplicity. The feedback signal in the circuit is connected to the non-inverting input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, a feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series RC network in one arm parallel RC network in the adjoining arm. Resisrors R_i and R_f are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge. The frequency of oscillation is the resonant frequency of the balanced bridge and is given by the expression $f_o = \frac{1}{2\pi RC}$. From the analysis of the circuit,it can be seen that the feedback factor $\beta = 1/3$ at the frequency of oscillation. Therefore, for the sustained oscillation,the amplifier must have a gain of 3.

Circuit diagram and waveforms:



With amplitude stabilization



Without amplitude stabilization

Design :

Without amplitude stabilization

Required frequency, $f_o = \ldots$ kHz.

Given $f_o = \dfrac{1}{2\pi RC}$.

Let $C = \ldots$ μF. $R_1 = R_2 = R = \ldots$ kΩ.

Use $\ldots$ kΩ std.

Gain $1 + \dfrac{R_f}{R_i} = 3$, Then $R_i = \ldots$ kΩ.

Then $R_3 = R_f = \ldots$ kΩ, use $\ldots$ kΩ potentiometer.

Select $R_4 = \ldots$ kΩ, and C_1 and $C_2 = \ldots$ μF.

With amplitude stabilization

Required frequency, fo= $\ldots$ kHz.

Given fo=1/(2πRC)

Let C=. . . .μF. R1=R2=R=. . . .k Use . . . ..k std. Gain 1+Rf/Ri=3, Then Ri=. . . .k.

Then R3= Rf=. . . ..k,use . . . .k potentiometer. Select Rs= . . . .M, and CS=. . . .μF

Procedure

1. Verify the conditions of op-amp and JFET.

2. Set up the circuit and observe the output waveform. Note down the frequency and amplitude of oscillation.

Results

Designed the wienbridge oscillator using op-amp with and without amplitude stabilization.32

EXPERIMENT NO. 11

Notch filters to eliminate the 50Hz power line frequency

Aim

Design and setup a notch filters to eliminate the 50Hz power line frequency.

Components Required

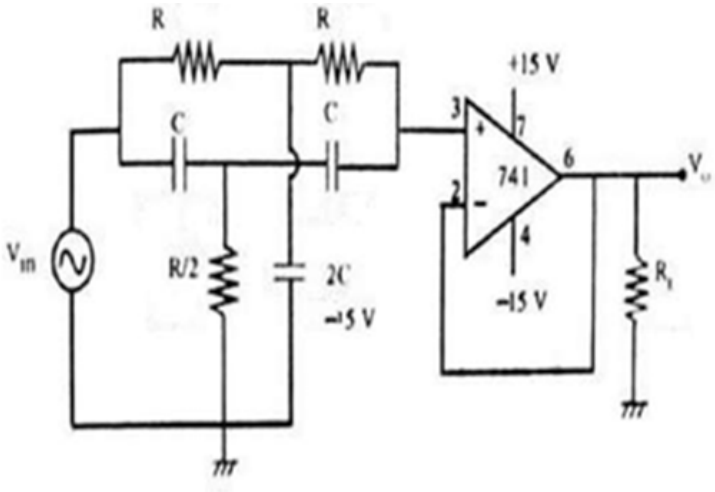
Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

Band elimination filter is also known as band rejection filter or band stop filter. Wideband rejection can be setup by connecting a low pass filter and a high pass filter in parallel. If an LPF with f_L is connected in parallel with HPF with f_H such that $f_H > f_L$, it forms BEF with bandwidth $f_H - f_L$.

Narrow band rejection filter is also known as notch filter. It provides maximum attenuation at f0. This is achieved by a twin-T RC network. Passive twin T network has relatively low figure of merit Q. Q can be increased by associating with a voltage follower using op amp. Notch filter has wide applications in communication field. It is used to eliminate undesired frequencies. The very common application is to remove power supply that access at 50 Hz.

Circuit diagram:



Design :

Required notch frequency $f_N = \dfrac{1}{2\pi RC} = \ldots$ KHz

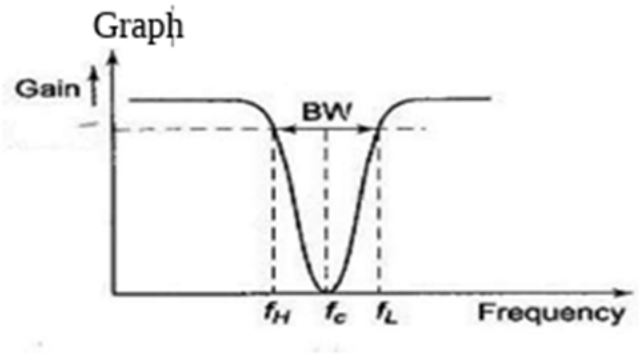
Take $C = \ldots$ μF. Then $R = \ldots$ K.

Take $2C = \ldots$ 1 μF and $R/2 = \ldots$ K.

Tabular Column $V_{in} = \ldots$ volt

f (Hz)	V_0 (V)	Log(f)	A_v in dB

Graph



Procedure

1. Set the signal generator output as . . . ..V sine wave
2. Vary the frequency of sine wave and note down the output voltage.
3. Plot the frequency response on graph sheet.

Results

Designed a notch filters to eliminate the 50Hz power line frequency.

Cycle II: Analog Integrated Circuits Lab

EXPERIMENT NO. 12

Astable and Monostable Multivibrator using NE555

Aim

To study NE555 Timer and to design and setup an astable multivibrator and monostable multivibrator using NE555 timer for a frequency of 1KHz.

Components Required

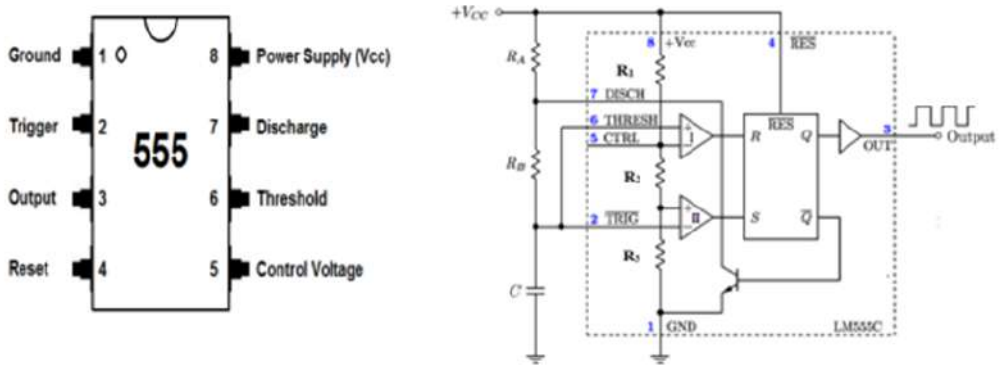
NE555 timer, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation introduced this device as SE555/NE555 in 1971. The 555 timer is available with the supply voltage between +4.5 to +18v, supply current 3 to 6 mA. It is compatible with both TTL and CMOS logic circuits. The functional block diagram of 555 consist of two comparators, a flip-flop, an output stage, two BJT Q1 and Q2 and a voltage divider network. The comparators are devices whose outputs are HIGH when the positive (+) input voltage is greater than the negative (-) input voltage and LOW when the negative (-) input voltage is greater than positive (+) input voltage. The voltage divider consisting of three 5KΩ resistors provide a trigger level of 1/3VCC and a threshold level of 2/3VCC. The control voltage input can be used externally adjust the trigger and threshold levels to other values, if necessary. When the normally HIGH trigger input momentarily goes below 1/3VCC, the output of comparator 2 switches from LOW to HIGH and set the S-R flip flop, causing the output to go HIGH and turning the discharge transistors Q1 OFF. The output will remain HIGH until the normally LOW threshold input goes above 2/3VCC and causes the output of comparator 1 to switch from LOW to HIGH. This resets the flip flop, causing the output to go back LOW and turning the discharge transistor ON. The external reset input can be used to reset the flip flop independent of threshold circuit. The

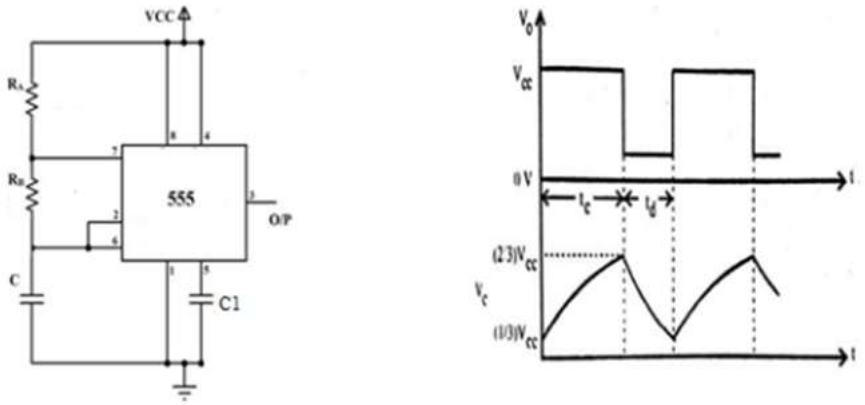
trigger and threshold inputs are controlled by external components connected to produce either monostable or astable action. So the output of timer becomes HIGH when the trigger input voltage is less than 1/3VCC and the output becomes LOW when the threshold voltage is greater than 2/3VCC. Also in stable state, the output of timer is LOW. Astable multivibrator: When the power supply VCC is connected, the external timing capacitor 'C" charges towards VCC with a time constant (RA+RB) C. During this time, pin 3 is high (VCC) as Reset R=0, Set S=1 and this combination makes Q =0 which has unclamped the timing capacitor 'C'. When the capacitor voltage equals 2/3 VCC, the upper comparator triggers the control flip flop on that Q =1. It makes Q1 ON and capacitor 'C' starts discharging towards ground through RB and transistor Q1 with a time constant RBC. Current also flows into Q1 through RA. Resistors RA and RB must be large enough to limit this current and prevent damage to the discharge transistor Q1. The minimum value of RA is approximately equal to VCC/0.2. During the discharge of the timing capacitor C, as it reaches VCC/3, the lower comparator is triggered and at this stage S=1, R=0 which turns Q =0. Now Q =0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 VCC and 1/3 VCC respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 VCC to 2/3 VCC. The charging period of capacitor = 0.69 (RA + RB) C. The discharging period of capacitor = 0.69 RB C. Monostable multivibrator: A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode Q is high and in turn, Q1 is turned ON and output is low. When the negative going trigger passes through VCC/3, the FF is set i.e. Q =0. This makes transistor Q1 off. The capacitor starts charging towards VCC, which was earlier clamped to zero. After a time period, the capacitor voltage becomes greater than 2/3 VCC and upper comparator resets the FF, i.e. R=1, S=0. This makes Q =1. In turn the transistor Q1 turns ON and thereby discharging the capacitor C rapidly to ground potential. Mononostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low.

Circuit diagram and waveforms:

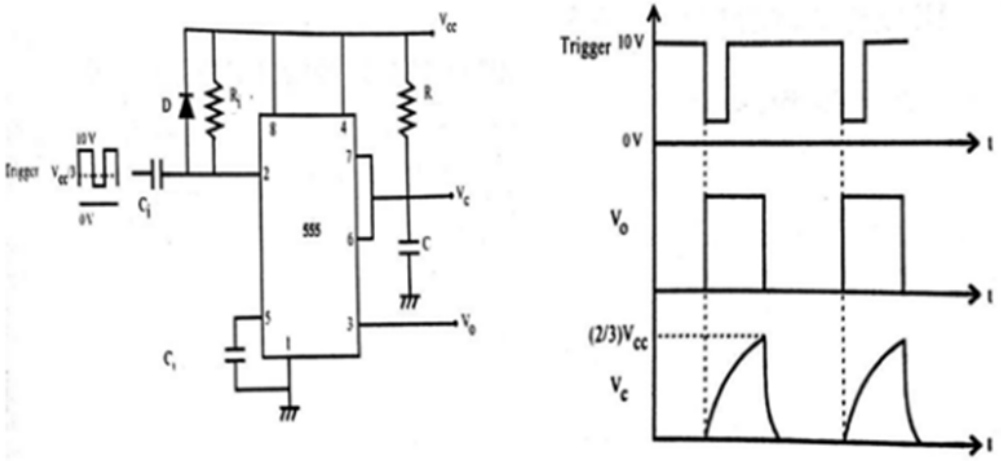


Pin out of 555 timer IC and Functional block diagram of 555 timer

Astable multivibrator using 555 timer



Monostable multivibrator using 555 timer



Design :

1. Astable multivibrator

   Take $V_{CC} = \ldots$ V and $t_c = \ldots$ ms and $t_d = \ldots$ ms. We have, $t_c = 0.69(R_A + R_B)C$ and $t_d = \ldots R_B$. The R_A and R_B should be in the range of 1K to 10K to limit the collector current of the internal transistor. Take $R_A = R_B = \ldots$ KΩ. Let $C = \ldots$ μF. Choose $C_1 = \ldots$ μF.

2. Monostable multivibrator

   Take $V_{CC} = \ldots$ V and $T = \ldots$ ms. We have, $T = \ldots RC$. Take $R = \ldots$ KΩ to limit current through the internal transistor to $\ldots$ mA. Then $C = \ldots$ μF.

   Design of triggering circuit: we have $R_i C_i \leq 0.0016 T_t$ where T_t is the time period of the trigger. Take $T_t = \ldots$ ms. Take $R_i = \ldots$ KΩ to avoid loading. Then $C_i = \ldots$ μF. Choose $C_1 = \ldots$ μF.

Procedure

1. Set up the astable multivibrator circuit after verifying the condition of the IC.
2. Observe the output waveform at pin no. 3 and 6 of the IC.
3. Set up the monostable multivibrator circuit.
4. Use positive pulses of amplitude V_{CC} and frequency $\ldots$ Hz as the trigger.

5. Observe the output waveform at pin no. 3 and 6 of the IC.

Results

Familiarized the NE555 Timer and designed an astable multivibrator and monostable multivibrator using NE555 timer for a frequency of 1KHz.

EXPERIMENT NO. 13

DC power supply using IC 723

Aim

To design and set up a low voltage and a high voltage regulator using IC RC723.

Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

723 is a general-purpose regulator that can be adjusted over a wide range of both positive and negative regulated voltage. It has two sections 1- a Zener diode, a constant current source and a reference amplifier that produces a fixed voltage of 7.15 at the terminal Vref.. The constant current source forces the Zener to operate at a fixed point so that the Zener outputs a fixed voltage. 2- it consists of an error amplifier; a series pass transistor Q1 and a current limiting transistor Q2. The error amplifier compares a sample of the output voltage applied at the INV input terminal. The error signal controls the conduction of Q1. These two sections are not internally connected but various points are brought out on the IC package.723 regulator IC are available in a 14-pin dual in line package or 10 pin metal can. It is inherently a low current device, but it can be boosted to provide 5A or more current by connecting external components. But it has no built-in thermal protection. It also has no short circuit current limits. It can operate with an input voltage from 9.5V to 40V and provide output voltage from 2V to 37V.

Low voltage regulator: A positive low voltage regulator using 723 is as shown. The voltage at NI terminal of the error amplifier due to R1R2 divider is VIN= Vref(R2/R1+R). The differences between VIN and the output voltage V0 is directly fed back to the INV terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q1 so as to minimize the difference the NI and INV input of error amplifier. Since Q1 is operating

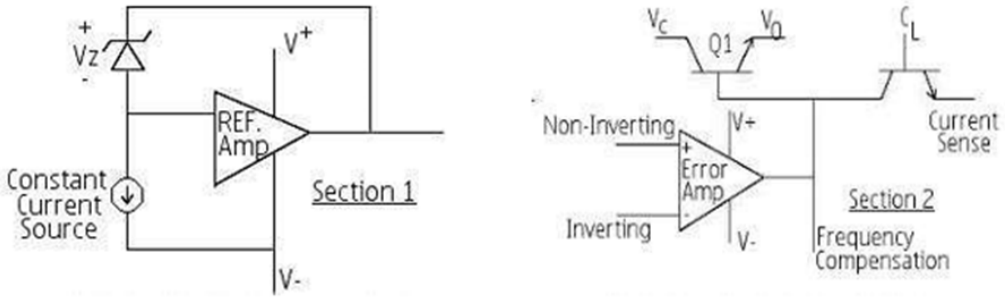
as an emitter follower V0=Vref(R2/R1+R2). If the output voltage becomes low, the voltage at the INV terminal of the error amplifier also goes down. This makes the output of the error amplifier to become more positive, thereby driving transistor Q1 more into conduction. This reduces the voltage across Q1 and drive more current into the load causing the voltage across the load to increase. So the initial drop in the load voltage has been compensated. Similarly, any increase in load voltage, or changes in the input voltage get regulated. The reference voltage typically 7.15volt, so the output voltage V0=7.15(R2/R1+R2). This will be always being less than 7.15V.

High voltage regulator:

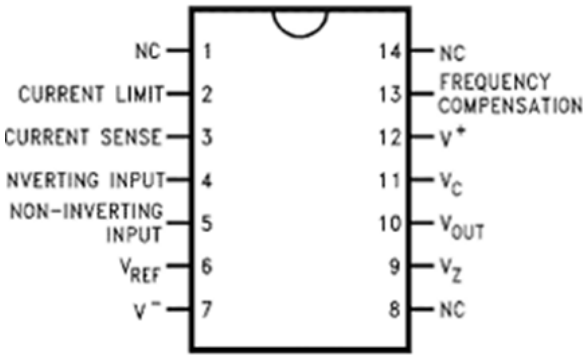
If it is desired to produce regulated output voltage greater than 7V, a small change should be made in the circuit for low voltage regulator. The non-inverting terminal is connected directly to Vref through R3. So, the voltage at the non-inverting terminal is Vref. The error amplifier operates as a non-inverting amplifier with a voltage gain of $A_v = 1 + \frac{R1}{R2}$. Notice that A_v is always greater than 1. So, the output voltage of the circuit is $V_o = 7.15\left(1 + \frac{R1}{R2}\right)$.

Circuit diagram:

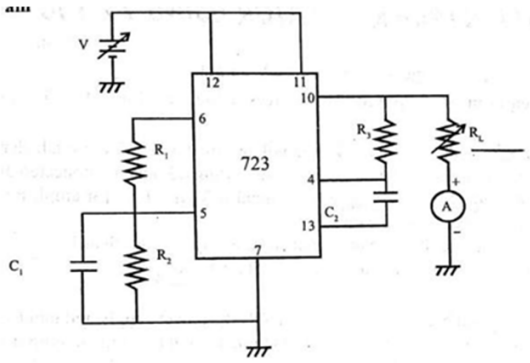
Functional block diagram of 723 regulator



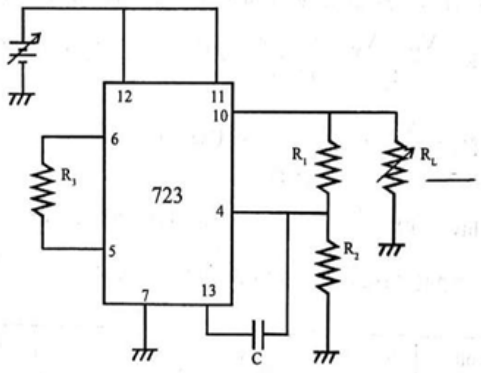
Pin diagram of IC 723



Low voltage regulator



High voltage regulator



Design :

Low voltage regulator

$V_0 = \frac{R_2}{R_1+R_2} = \ldots V \quad V_{\text{ref}} = \ldots V$

$R_1 = \frac{V_{\text{ref}}-V_0}{I_D} = \frac{7.15-6}{1\text{ mA}} = \ldots\ \text{k}\Omega$

$V_0 = \ldots V \quad R_2 = \frac{V_0}{I_D} = \frac{6\text{ V}}{1\text{ mA}} = \ldots\ \text{k}\Omega \approx \ldots\ \text{k}\Omega$

$I_D = \ldots\ \text{mA}$

Take $C = \ldots\ \text{pF} \quad R_3 = \ldots\ \text{k}\Omega$

High voltage Regulator

$V_0 = 7.15\left(1 + \frac{R_1}{R_2}\right)$

Take $R_1 = \ldots\ \text{k}\Omega$

$1 + \frac{R_1}{R_2} = \frac{12}{7.15} \quad R_2 = \ldots\ \text{k}\Omega$

Use $R_2 = \ldots\ \text{k}\Omega$ std

$C = \ldots\ \text{pF}$ Take $R_L = \ldots\ \Omega$ rheostat

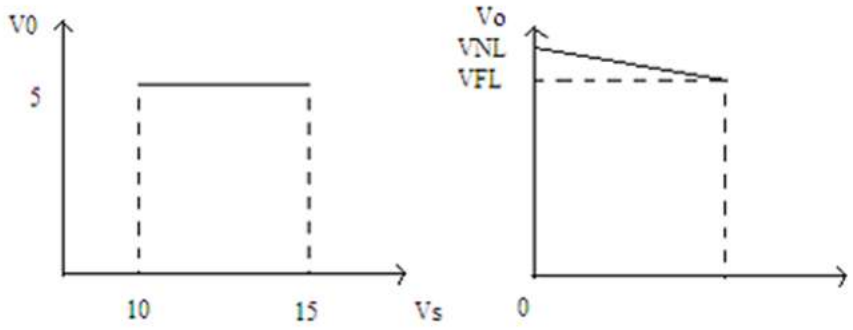
Low voltage regulator

Observations:

Line Regulation Measurements	
V_s (V)	V_o (V)
10	
11	
12	
13	
14	
15	

Load Regulation Measurements	
I_L (mA)	V_o (V)
0	
5	
10	
20	
40	
70	
80	
100	

Typical graph



Line regulation Load Regulation

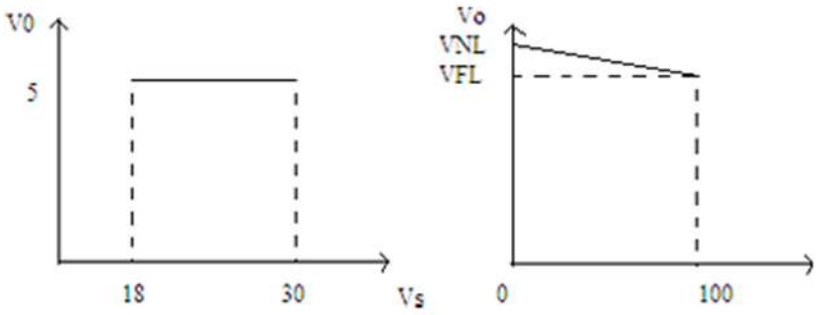
High voltage regulator

Observations:

Line Regulation Measurements	
V_s (V)	V_o (V)
18	
20	
22	
24	
28	
30	

Load Regulation Measurements	
I_L (mA)	V_o (V)
0	
5	
10	
20	
40	
70	
80	
100	

Typical graph



Procedure

Low voltage regulator:

1. Set up the circuit. Switch on the power supply and input voltage sources.
2. Vary the input voltage from . . . .V to . . . .V and observe the output voltage. Note down it in tabular column.
3. Vary the rheostat and note the change in output current.
4. Draw the regulation characteristics with input on X-axis and output on Y-axis.
5. Calculate the % line regulation using the expression:

$$S_V = \frac{\text{change in output voltage}}{\text{change in input voltage}}$$

6. Calculate the % load regulation using the expression:

$$S_L = \frac{V_{NL} - V_F}{V_{NL}}$$

High voltage regulator:

1. Set up the circuit. Switch on the power supply and input voltage sources.
2. Vary the input voltage from . . . .V to . . . ..V and observe the output voltage. Note down it in tabular column.

3. Vary the rheostat and note the change in output current.

4. Draw the regulation characteristics with input on X-axis and output on Y-axis.

Results

Designed the voltage regulator circuits using IC 723. Load regulation for:

- Low voltage regulator = ...
- High voltage regulator = ...

EXPERIMENT NO. 14

A/D converters- counter ramp and flash type.

Aim

To design and setup a counter ramp and flash type ADC.

Components Required

Op-amp, diode, resistors, capacitors, comparator LM311, IC's 7408,7493,741, breadboard, CRO, function generator and power supplies.

Theory

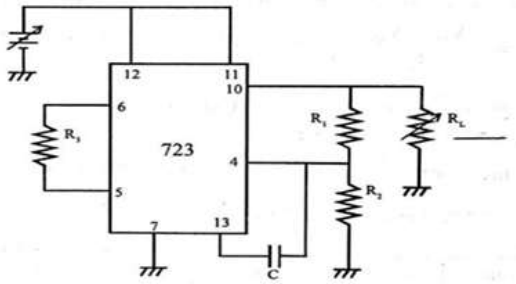
Counter ramp ADC: It displays the digital equivalent of input analog signal. Basically, a comparator opens a gate for a period of time and a counter counts the number of pulses flowing through the gate. Comparator keeps the gate open until the analog equivalent of the digital output of the counter equals the input voltage that to be digitized.

A four-bit binary counter 7493 is used to count the pulses. An op amp with R-2R ladder network is used as a digital to analog converter. Comparator output provides high output as long as $V_{in} > V_a$. V_{in} is the input to be digitized and V_a is the analog equivalent of the instantaneous digital output. When $V_{in} < V_a$, gate closes and pulses stop to flow to binary counter. Digital output remains standstill at its value.

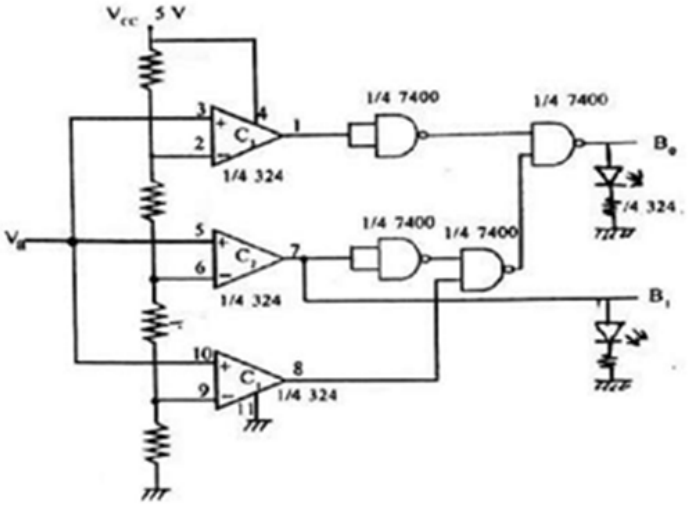
2-bit flash ADC: If the analog signal exceeds the reference signal to any comparator, that comparator turns on. If all comparators are off, analog input will be between 0 and $+V/4$. If C1 is high and C2 and C3 are low, input will be between $+V/4$ and $+V/2$. If C1 and C2 are high and C3 is low, input will be between $+V/2$ and $+3V/4$. If all comparators are high, analog input will be between $+3V/4$ and $+V$. The outputs of three comparators are then fed to a coding network to provide 2 bits which are equivalent to the input analog voltage.

Circuit diagram:

Counter ramp ADC



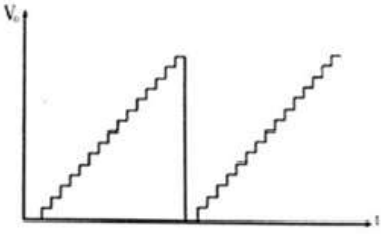
2 bit FLASH ADC



Tabular column

V (Volts)	S_3	S_2	S_1	S_0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

Waveform



Procedure

1. Set up the circuit for counter ramp ADC and . . . ..bit flash ADC.

2. Vary the analog input from . . . ..V to . . . . . .V and observe the output bits.

Results

Designed and setup the ADC circuits.

EXPERIMENT NO. 15

Study of PLL IC: free running frequency lock range capture range

Aim

To design set up a PLL circuit and study its functional characteristics.

Components Required

565 PLL IC, Power Supply, Function generator, CRO, Resistors, Capacitors, Bread board

Theory

PLL is a control system that generates an output signal whose phase is related to the phase of input reference signal. It mainly consists of a phase detector, an LPF and a VCO. Phase comparator or phase detector compare the frequency of input signal f_s with frequency of VCO output f_o and it generates a signal which is function of difference between the phase of input signal and phase of feedback signal which is basically a d.c voltage mixed with high frequency noise. LPF remove high frequency noise voltage. Output is error voltage. If control voltage of VCO is 0, then frequency is center frequency (f_o) and mode is free running mode. Application of control voltage shifts the output frequency of VCO from f_o to f. On application of error voltage, difference between f_s & f tends to decrease and VCO is said to be locked. While in locked condition, the PLL tracks the changes of frequency of input signal.

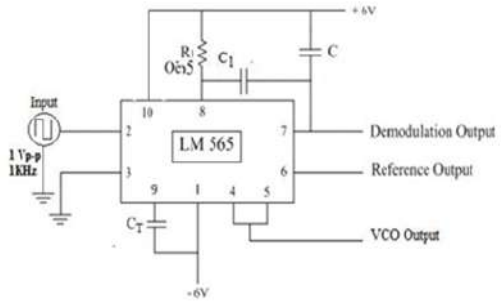
Center frequency (free running frequency) $f_o = \frac{1.2}{4R_1C_1}$ Hz

Lock range $f_L = \pm\frac{8f_o}{V}$ Hz

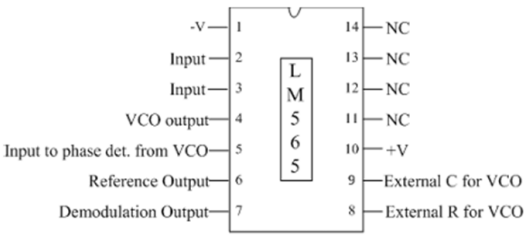
Capture range $f_c = \pm\left[\frac{f_L}{2\Pi(3.6)x10^3\, xC2}\right]^{1/2}$

Circuit diagram:

Block diagram of 565 PLL and Pinout

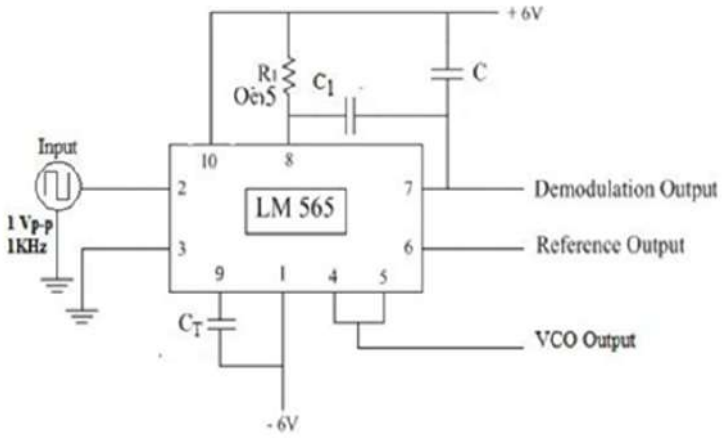


Block Diagram of 565 PLL

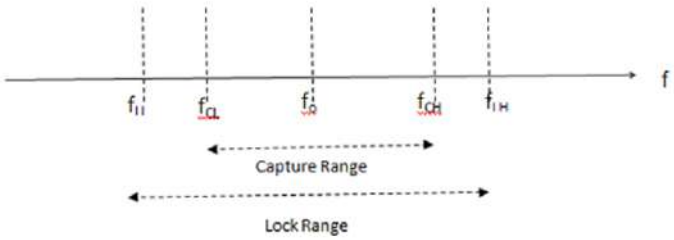


Pinout of 565 PLL

Circuit diagram of PLL



Graph



Design :

Take $V_+ = \ldots$ V and $V_- = \ldots$ V. Let the free running frequency f_0 be 2.5 kHz = $\frac{1.2}{4R_1C_1}$. Take $C_1 = \ldots \mu$F. Then $R_1 = \ldots$ kΩ. The value of R_1 satisfies the required condition $2k < R_2$. Take $C_3 = \ldots \mu$F, $C_2 = \ldots \mu$F. Then the theoretical values of f_L and f_C are:

$$f_L = \pm\frac{8 \cdot 2.5 \cdot 10^3}{10 - (-10)} = \ldots \text{ kHz}$$

$$f_C = \frac{\sqrt{10^3}}{\sqrt{2\pi \cdot 3.6 \cdot 10^3 \cdot 10 \cdot 10^{-6}}} = \ldots \text{ Hz}$$

Procedure

1. Verify the condition of components.
2. Set up the circuit and observe the output waveform and note down the VCO frequency.
3. Feed a square wave to the pin no.2 of 565 PLL IC and vary its frequency from ... Hz to ... MHz and note down f_{C1} and f_{L2}. Then decrease the frequency from ... MHz to ... Hz and note down f_{C2} and f_{L1}.
4. Calculate capture range and lock range.

Results

Designed the PLL IC and obtain the results.

Free running frequency: .....

Capture range: .....

Lock range: .....

EXPERIMENT NO. 16

D/A Converters- ladder circuit

Aim

To design and set up a R-2R ladder type DAC.

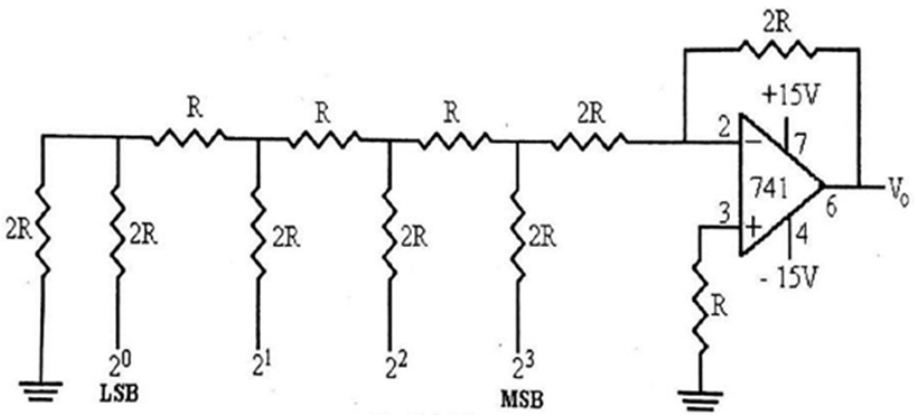
Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory

An R-2R ladder DAC uses fewer unique resistor values. Only two resistance values are used anywhere in the entire circuit. This means that only two values of resistance in the ratio 2:1. Current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same, so the incoming current splits equally along both paths. The half current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along the ladder can affect the output.

Circuit diagram:

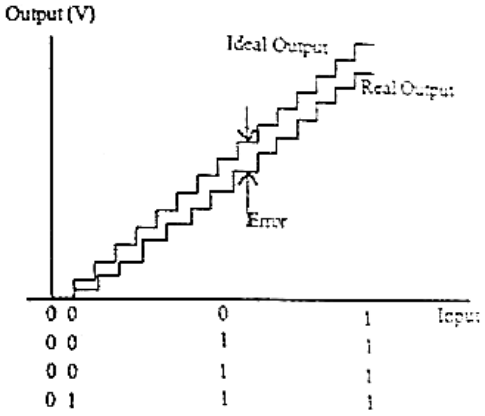


Design :

Let R = . . . kΩ and $2R$ = . . . kΩ

Observations and typical response curve

Q3 Q2 Q1 Q0	V0 (Volts)
0000	
0001	
0010	
. . .	
. . .	
1101	
1110	
1111	



Procedure

1. Verify the conditions of the op-amp.
2. Set up the DAC circuit and manually enter binary inputs from . . . .. to . . . .
3. Measure the output voltage using a multimeter and tabulate the readings.
4. Draw the response with analog output on Y-axis and binary output on X-axis.

Results

Designed the ladder circuit DAC. Error in the output = ...%

Cycle III: Analog Integrated Circuits Lab

EXPERIMENT NO. 17

DIFFERENCE AMPLIFIER AND INSTRUMENTATION AMPLIFIER

Aim

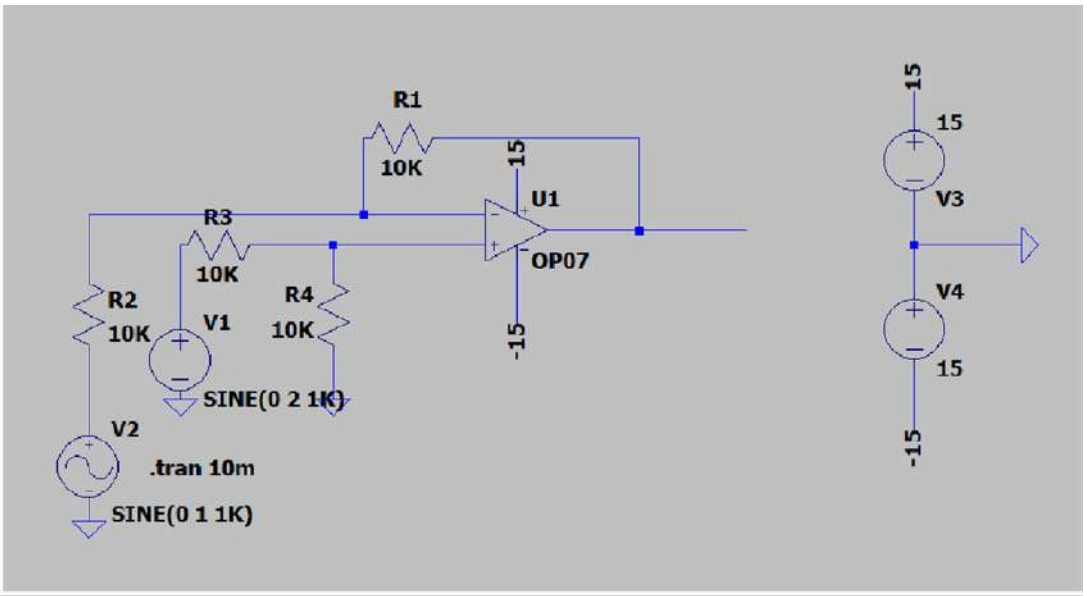
To design and simulate a difference amplifier and instrumentation amplifier using Op-amp in LtSpice and view the output waveform.

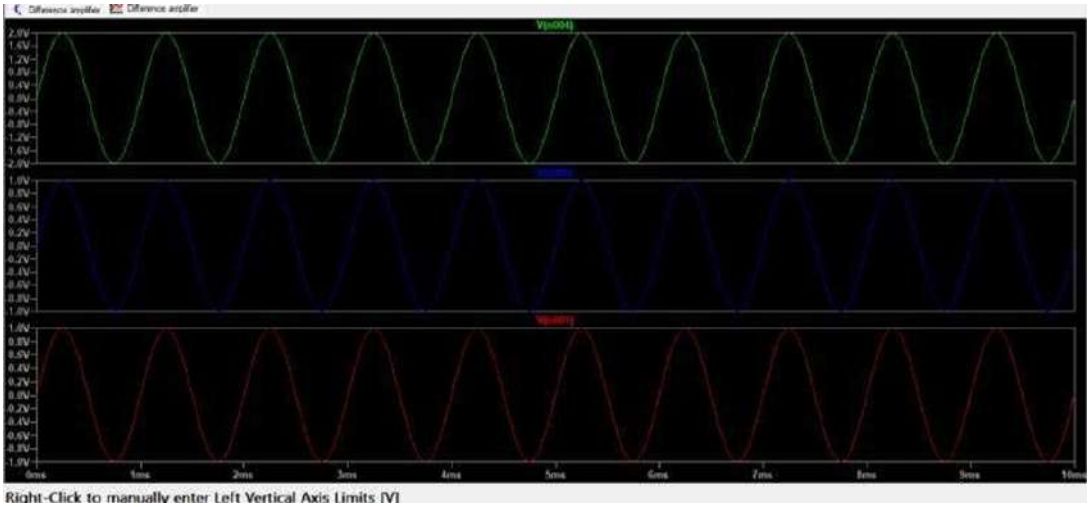
Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator power

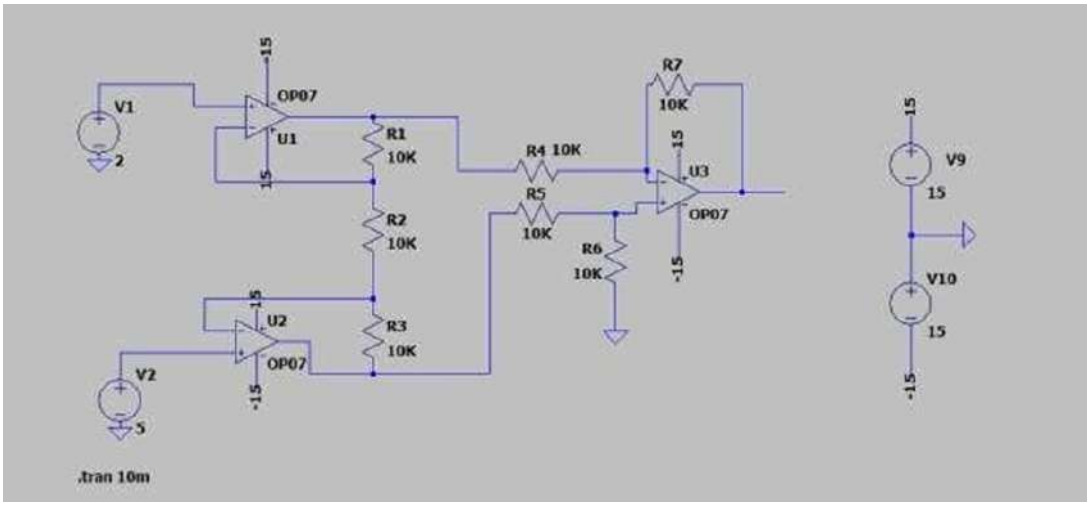
Circuit diagram and waveforms:

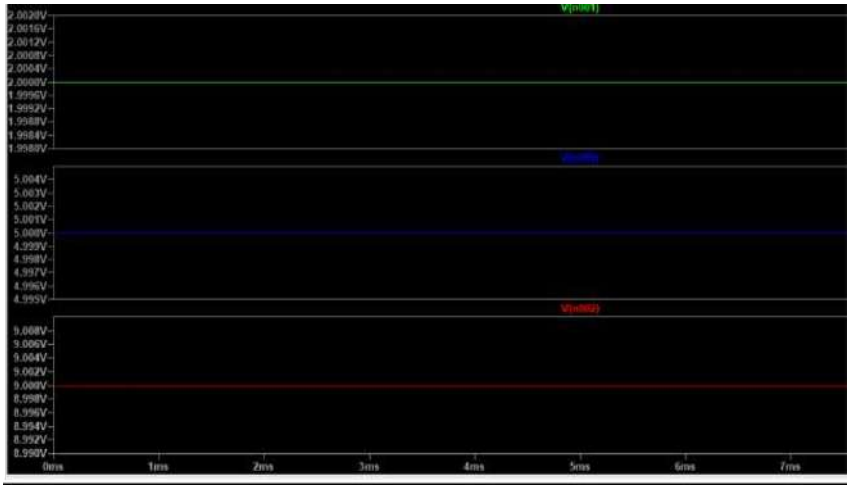
Difference amplifier





Instrumentation amplifier





Procedure

1. Open LTspice, start a new schematic, and set up the workspace.
2. Go to the component library to add necessary components (e.g., resistors, capacitors, voltage sources) and place them on the schematic.
3. Label key nodes by right-clicking on wires and naming points (e.g., N001, N002) for clarity.
4. Set component values by right-clicking on each component and entering its value (e.g., resistance, capacitance, voltage).
5. Use the wire tool to connect components according to the circuit diagram.
6. Right-click on the schematic background, and enter the simulation command for the desired analysis type.
7. Click the Run button to begin the simulation, opening the waveform viewer to display results.
8. Place probes by clicking on specific nodes or components to observe voltage or current at those points.
9. Record readings and observations, noting peak values, response times, and steady-state values.
10. Compare observed results with theoretical values, calculating key parameters as required.

Results

Designed and Simulated difference amplifier and instrumentation amplifier and verified the output waveform.

Instrumentation Amplifier A_c = ...

A_d = ...

CMRR = . . . dB

EXPERIMENT NO. 18

Waveform generators using Op-amps – Triangular and Sawtooth

Aim

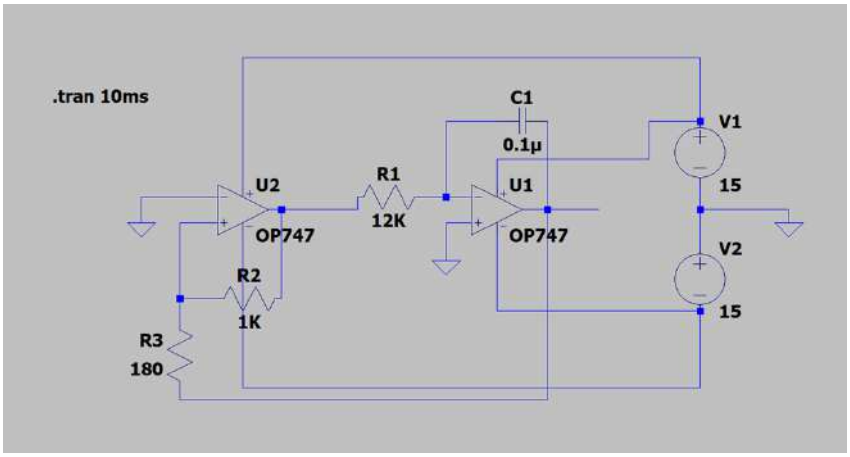
To set up and simulate a saw-tooth and triangular wave form generator using Op-Amp for 1KHz frequency and view the output waveform

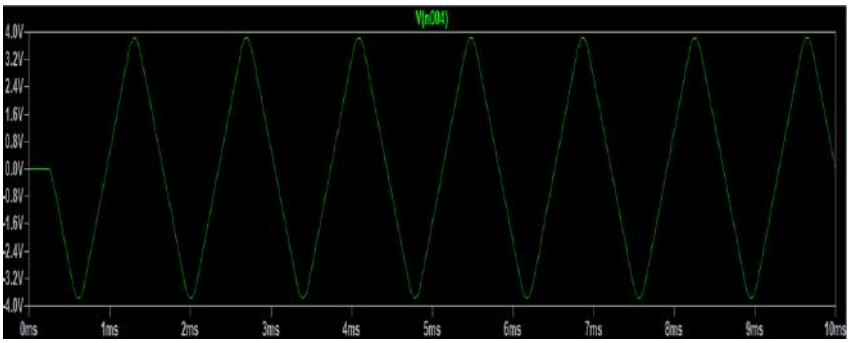
Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

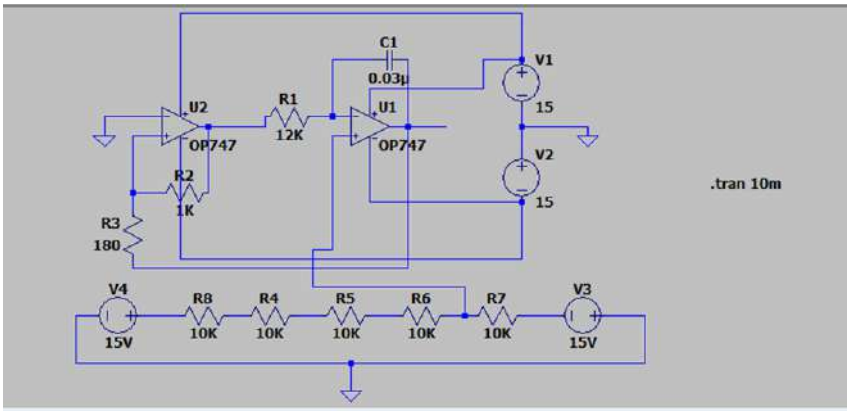
Circuit diagram and waveforms:

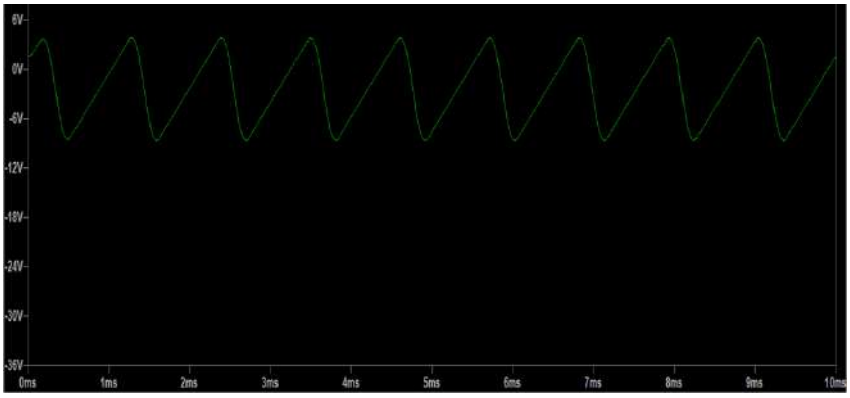
Triangular wave generator





Sawtooth wave generator





Procedure

1. Open LTspice, start a new schematic, and set up the workspace.
2. Go to the component library to add necessary components (e.g., resistors, capacitors, voltage sources) and place them on the schematic.
3. Label key nodes by right-clicking on wires and naming points (e.g., N001, N002) for clarity.
4. Set component values by right-clicking on each component and entering its value (e.g., resistance, capacitance, voltage).
5. Use the wire tool to connect components according to the circuit diagram.
6. Right-click on the schematic background, and enter the simulation command for the desired analysis type.

7. Click the Run button to begin the simulation, opening the waveform viewer to display results.
8. Place probes by clicking on specific nodes or components to observe voltage or current at those points.
9. Record readings and observations, noting peak values, response times, and steady-state values.
10. Compare observed results with theoretical values, calculating key parameters as required.

Results

Designed and simulated a triangular wave and saw tooth wave generator using op-amp.

Triangular Wave Generator

V_{pp} = ...V,

F = ...KHz

Sawtooth Wave Generator

V_{pp} = ...V,

F = ...KHz

T_{rise} = ...ms,

T_{fall} = ...ms,

T_{period} = ...ms

EXPERIMENT NO. 19

Active second order filters using Op-amps– HPF,LPF,BPF,BSF

Aim

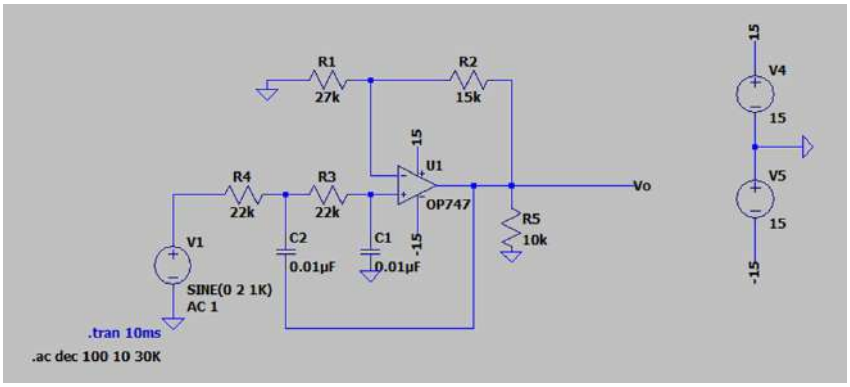
To design and set up the active second order filters using op amp.

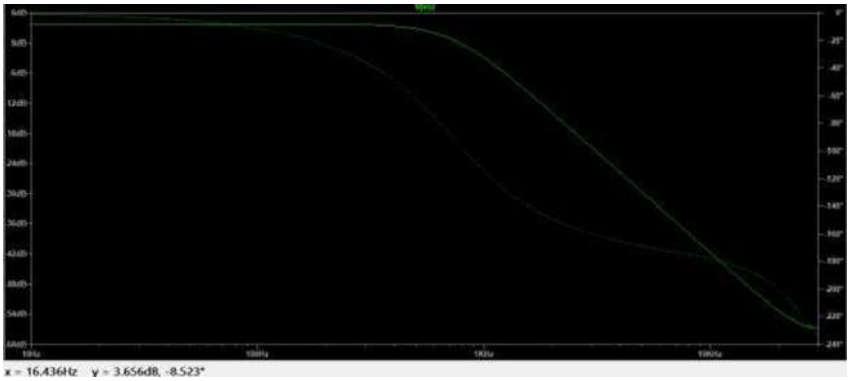
Components Required

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

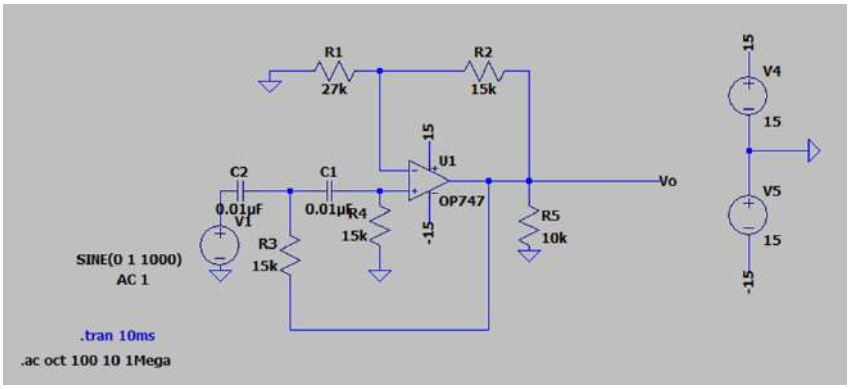
Circuit diagram and waveforms:

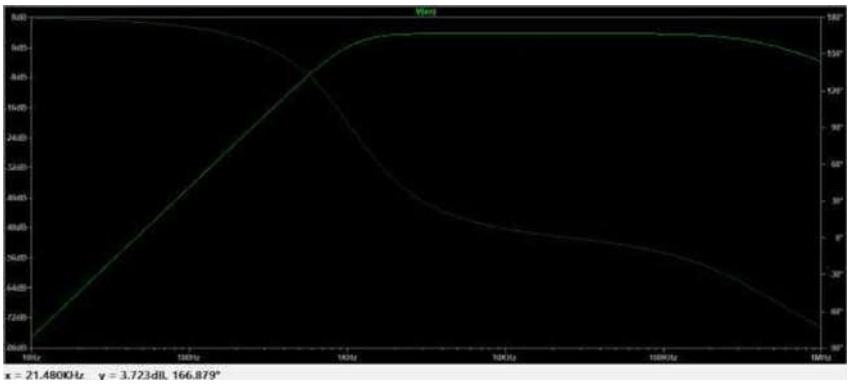
Active low pass filter



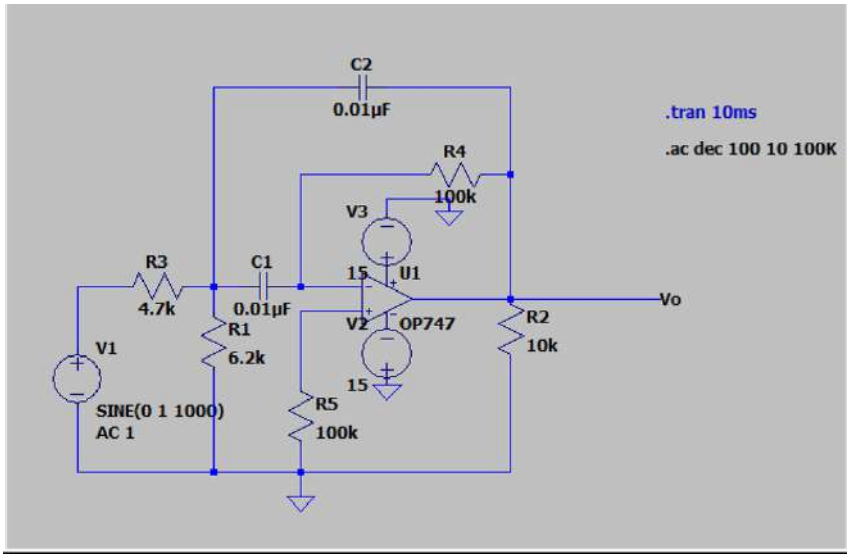


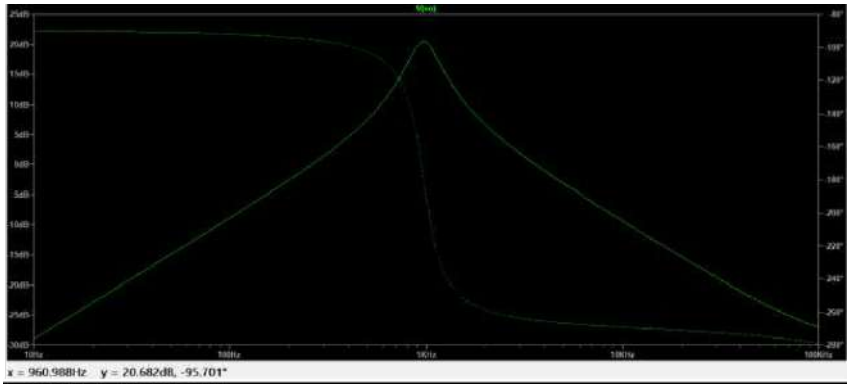
Active high pass filter



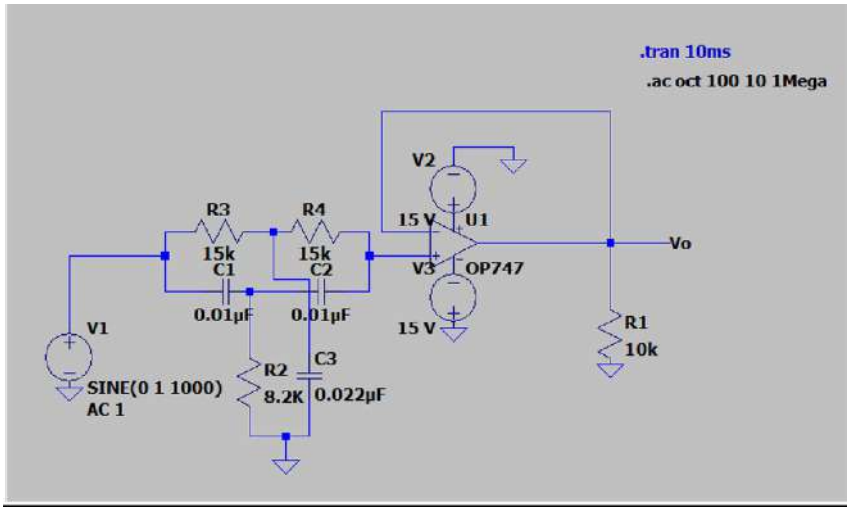


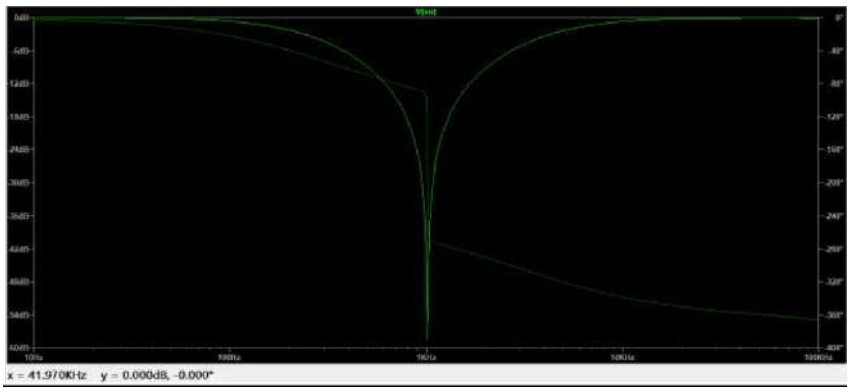
Active bandpass filter





Active band stop filter





Procedure

1. Open LTspice, start a new schematic, and set up the workspace.
2. Go to the component library to add necessary components (e.g., resistors, capacitors, voltage sources) and place them on the schematic.

3. Label key nodes by right-clicking on wires and naming points (e.g., N001, N002) for clarity.
4. Set component values by right-clicking on each component and entering its value (e.g., resistance, capacitance, voltage).
5. Use the wire tool to connect components according to the circuit diagram.
6. Right-click on the schematic background, and enter the simulation command for the desired analysis type.
7. Click the Run button to begin the simulation, opening the waveform viewer to display results.
8. Place probes by clicking on specific nodes or components to observe voltage or current at those points.
9. Record readings and observations, noting peak values, response times, and steady-state values.
10. Compare observed results with theoretical values, calculating key parameters as required.

Results

Designed and simulated active low pass filter, high pass filter, bandpass filter and bandstop filter using op-amp and verified the output waveform.

Gain of low pass filter = ... dB

Gain of high pass filter = ... dB

Band pass filter:

F_l = ... Hz

F_h = ... KHz

$F_c = \sqrt{F_l \cdot F_h}$ = ... Hz

Band stop filter:

F_l = ... Hz

F_h = ... KHz

$F_n = \sqrt{F_l \cdot F_h}$ = ... KHz

EXPERIMENT NO. 20

A/D converters- counter ramp and flash type.

Aim

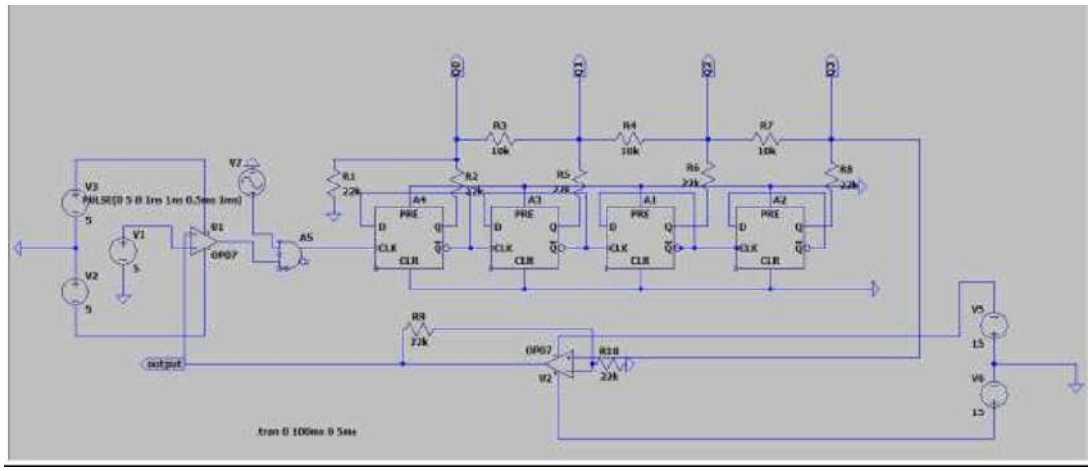
To design and setup a counter ramp and flash type ADC.

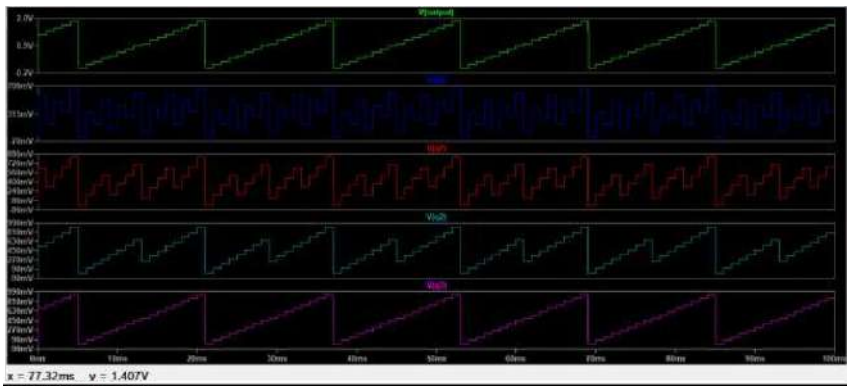
Components Required

Op-amp, diode, resistors, capacitors, comparator LM311,IC's 7408,7493,741, breadboard, CRO, function generator and power supplies.

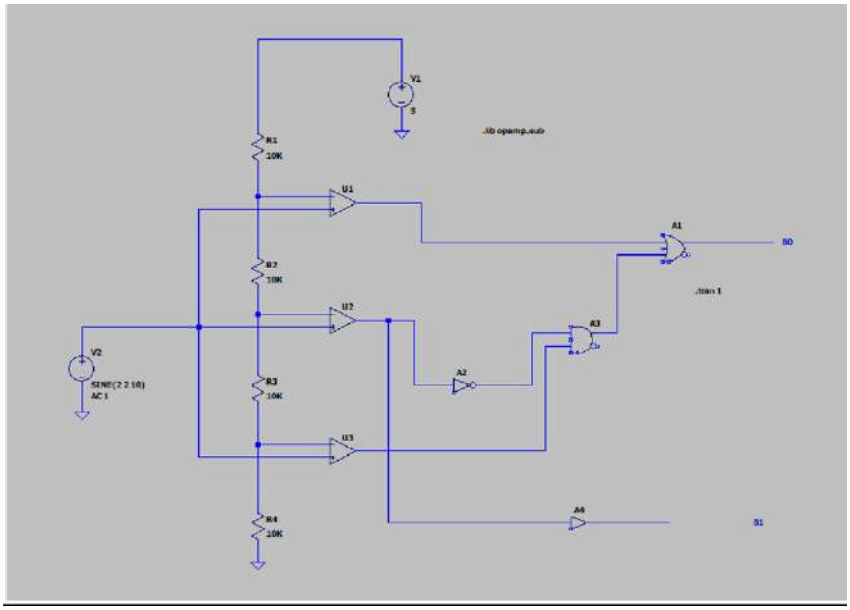
Circuit diagram and waveforms:

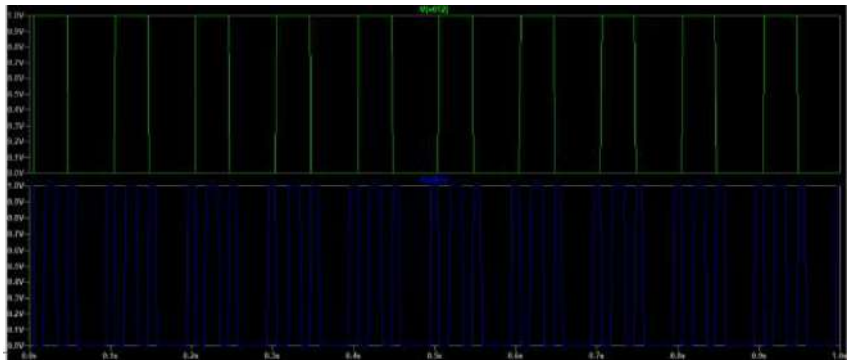
Counter ramp





Flash ADC





Procedure

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2. Go to the component library to add necessary components (e.g., resistors, capacitors, voltage sources) and place them on the schematic.
3. Label key nodes by right-clicking on wires and naming points (e.g., N001, N002) for clarity.
4. Set component values by right-clicking on each component and entering its value (e.g., resistance, capacitance, voltage).
5. Use the wire tool to connect components according to the circuit diagram.

6. Right-click on the schematic background, and enter the simulation command for the desired analysis type.
7. Click the Run button to begin the simulation, opening the waveform viewer to display results.
8. Place probes by clicking on specific nodes or components to observe voltage or current at those points.
9. Record readings and observations, noting peak values, response times, and steady-state values.
10. Compare observed results with theoretical values, calculating key parameters as required.

Results

Designed and simulated Analog to Digital converter flash type and counter ramp type and verified the output.