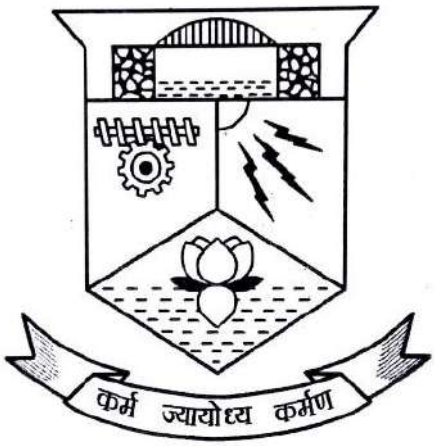
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
COLLEGE OF ENGINEERING, THIRUVANANTHAPURAM

Laboratory Manual

Of

COMMUNICATION ENGINEERING LAB (ANALOG & DIGITAL)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
COLLEGE OF ENGINEERING, TRIVANDRUM
2019

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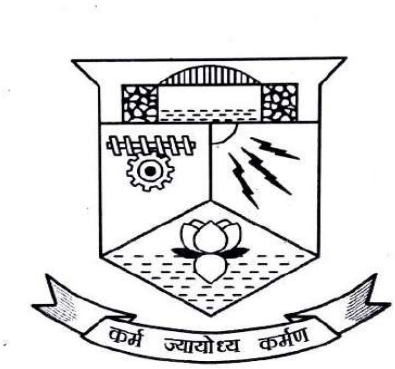

CERTIFICATE

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Head of Dept.

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CONTENTS:

1. AM GENERATION USING DISCRETE COMPONENTS

AIM:
To design and set up an AM generator using discrete components and measure the modulation index from the observed output waveform.

COMPONENTS AND EQUIPMENT REQUIRED:
High frequency transistors BF195, IFT, resistors, capacitors, Function generator, DC source and DSO.

THEORY:

Any amplifier can be converted into a sinusoidal oscillator if Barkhausen conditions are satisfied. So the tuned amplifier can be converted into a high frequency oscillator for generating carrier wave by providing a positive feedback after removing the input and the load resistor RL. In order to obtain the feedback signal to the base, the terminal-1 of the IFT primary coil is used. It is 180° out of phase with the signal at collector, ie. Terminal-2 of IFT primary winding. The collector signal is already 180° out of phase with the input signal at base of BJT. Thus the feedback signal from terminal-1 of the IFT to the base of BJT is in phase with the signal at the base. The feedback capacitor is chosen to be low to avoid additional phase shift. The circuit now works as an oscillator generating a signal of frequency of around 455kHz. Its amplitude, E_c can be adjusted by varying the potentiometer connected in series with the emitter resistance and frequency, f_c by tuning the IFT.

$$e_c = E_C \sin \sin ¿ \quad 2\pi f_c t)$$

The carrier thus generated can be modulated using an audio frequency message signal by connecting it at the emitter of the transistor. It can be of frequency varying from 1 KHz to 5 KHz. The amplitude can be varied in the range of 1 V to 10 V which changes the modulation index. The modulation index can also be varied by adjusting the carrier amplitude with the potentiometer connected at the emitter.

The ratio of the maximum amplitude of the modulating signal voltage to that of the carrier voltage is termed as modulation index. This is represented as $m = E_m / E_c$. For both carrier and message being sinusoidal, the modulation index will be $m = \frac{Emax - Emin}{Emax + Emin}$ where E_{max} and E_{min} are respectively the maximum and minimum height of the positive side of modulated signal.

DESIGN:

V_{CC} should be peak to peak output voltage swing + 20% peak to peak output voltage to compensate the inherent loss occurring at the coil's internal resistance.

Assume appropriate values of V_{CC}, V_{CE} and V_{EE}

To fix the Q point on the cut-off of the load line, take appropriate values of h_{FE} and $I_{C.}$

$V_{RE} = V_{CE} - V_{EE}$

Design of R_E

$V_{RE} = I_E R_E$

$\therefore R_E = \frac{V_{RE}}{I_E}$

Design of R_1& R_2

For the transistor to operate in class C region, assume that $V_{R2}=V_{RE}$.

So $V_{BE}=0V$; $V_{R2}=V_{RE}$ and the remaining voltage drops across R_1 i.e. V_{R1}

$$I_B = \frac{I_C}{h_{FE}}$$

$$R_2 = \frac{V_{R2}}{9 * I_B}$$

$$R_1 = \frac{V_{R1}}{10 * I_B}$$

Design of C_C:

Select suitable value of f_L.

$X_{C1} < R_{in}/10$

Input impedance is $R_{in}=R_1||R_2||(1+\beta)r_e$), where $r_e = \frac{V_T}{I_E}$

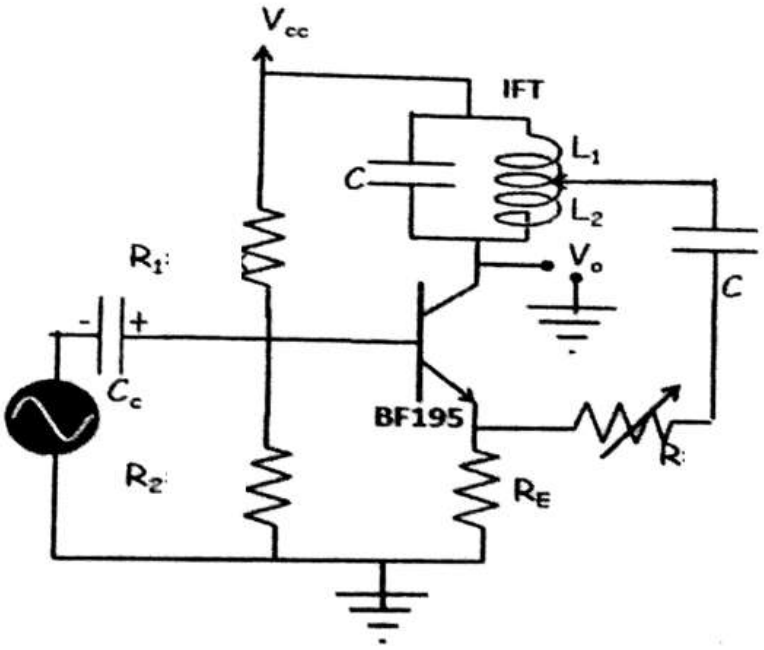
Then $C_{C1} > \frac{10}{(2\pi f_L Rin)}$

Take standard value of C_{C1} from the above relation.

Design of tuned circuit:

Use an IFT which is tuned to 500 KHz. Take appropriate values of R and C_C for tuning of feedback circuit.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Set up the carrier generator part of the circuit by adjusting the potentiometer.
2. Feed modulating signal (AF) and observe the AM signal on DSO.
3. Note down E_{max} and E_{min} of an AM signal and calculate modulation index.

2. AM USING MULTIPLIER IC AD633

AIM:
To design and implement AM generation and demodulation using multiplier IC AD633.

COMPONENTS AND EQUIPMENT REQUIRED:
Multiplier IC AD633, function generator, capacitor and DSO.

THEORY:

DSB-SC is same as AM devoid of the carrier. Inorder to obtain the complete AM waveform which is double side band with carrier, add the carrier signal to the DSB-SC signal. This can be done using the 633 multiplier IC.

$$W = \frac{XY}{10} + Z$$

$$W = \frac{Em\sin(2\pi fmt).Ec\sin(2\pi fct)}{10} + E_c\sin(2\pi fct)$$

$$W = \frac{EmEc[\cos(2\pi(fc-fm)t)]}{20} -$$

$$\frac{EmEc[\cos(2\pi(fc+fm)t)]}{20} + E_C\sin(2\pi f_c t)$$

The resultant AM can be demodulated in two ways,

1. Using Diode envelope detector.

2. Using another AD633 in cascade with AM generating circuit for multiplying the AM with the carrier.

Multiplying the AM with the carrier once again will result in the following output.

W=

$$\frac{1}{10}\left(\frac{EmEc[\cos(2\pi(fc-fm)t)]}{20}\right) - \frac{EmEc[\cos(2\pi(fc+fm)t)]}{20} + E_C\sin\sin(2\pi f_c t).E_C\sin(2\pi f_c t)$$

Thus, the signal consists of various frequencies of which, the smallest is the message frequency. It can be extracted by filtering using a low pass filter. Since the amplitude of the

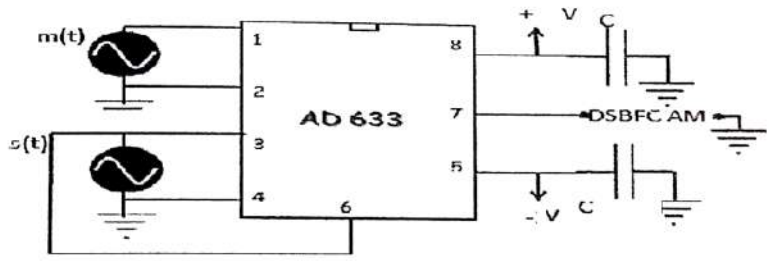
message frequency is very small, it may be amplified using a simple non-inverting amplifier using an op-amp.

PROCEDURE:

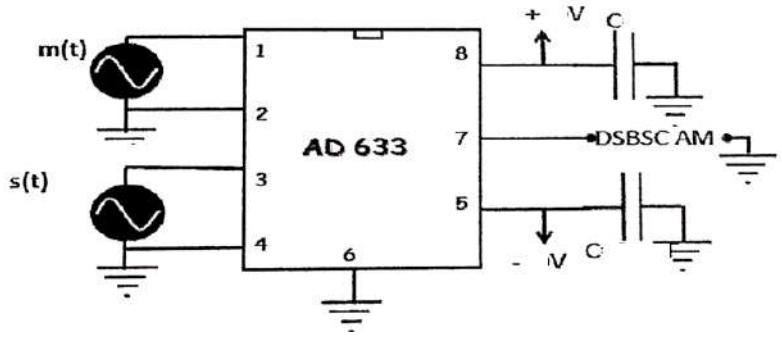
1. Set up classic AM circuit and feed sine wave carrier and modulating signals and observe the output waveform.
2. Set up the AM-DSBSC by modifying the previous circuits. Observe the output waveform and measure the modulation index.

CIRCUIT DIAGRAM:

AM-DSBFC:



AM-DSBSC:



3. AM DETECTION USING ENVELOPE DETECTOR

AIM:

To design and set up an AM detection system using envelope detector.

COMPONENTS AND EQUIPMENT REQUIRED:

Point contact diode OA79, capacitor, resistor, function generator, power supply and DSO.

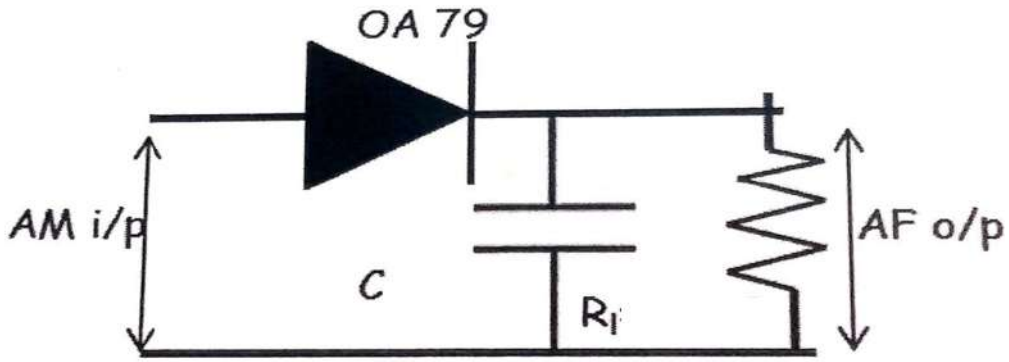
THEORY:

The process of detection provides a means of recovering the modulating signal from modulating signal. Demodulation is the reverse process of modulation. The detector circuit is employed to separate the carrier wave and eliminate the side bands. Since the envelope of an AM wave has the same shape as the message, independent of the carrier frequency and phase, demodulation can be accomplished by extracting envelope. An increased time constant RC results in a marginal output follows the modulation envelope. A further increase in time constant the discharge curve become horizontal if the rate of modulation envelope during negative half cycle of the modulation voltage is faster than the rate of voltage RC combination, the output fails to follow the modulation resulting distorted output is called as "diagonal clipping: this will occur even high modulation index. The depth of modulation at the detector output greater than unity and circuit impedance is less than circuit load (Rl > Zm) results in clipping of negative peaks of modulating signal. It is called 'negative clipping'.

The time constant of the circuit CR_L should be such that:

$$T_{carrier} << CR_L << T_{modulating}$$

CIRCUIT DIAGRAM:



DESIGN:

The time constant of the circuit should be:

$$T_{carrier} << CR_L << T_{modulating}$$

Choose appropriate values for $T_{modulating}$ and $T_{carrier}$, then

$CR_l = 10.T_{carrier}$

Choose appropriate value of C.

Then, find $R_l = \frac{10.T\,carrier}{C}$

PROCEDURE:

1. Set up the circuit after verifying the components.
2. Feed AM signal and observe the output.
3. Measure the output amplitude using DSO.

4. IF TUNED AMPLIFIER

AIM: To design and implement a tuned frequency amplifier using an IFT and to obtain its frequency response and calculate its Q-factor.

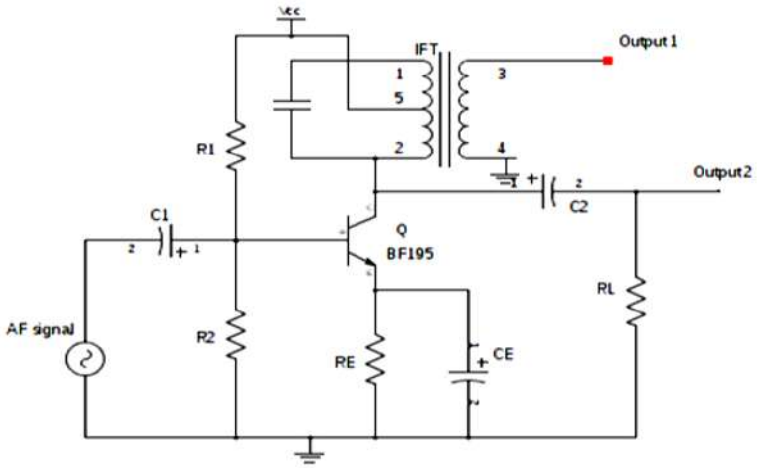
COMPONENTS AND EQUIPMENT:

BF495, IFT, resistors, capacitors, function generators, power supply and DSO.

THEORY:

Intermediate frequency amplifiers are tuned voltage amplifiers used to amplify a particular frequency. Its primary function is to amplify only the tuned frequency with maximum gain and reject all other frequencies above and below this frequency. These types of amplifiers are widely used in intermediate frequency amplifiers in AM super heterodyne receivers, where intermediate frequency is usually 455 kHz. In common emitter voltage amplifier circuit (emitter bypassed), the voltage gain is $AV = (RC||RL)/r_e$, where RC is the collector resistance in the circuit, RL is the load resistance and re is the internal emitter resistance. In tuned voltage amplifier the collector resistance is replace by a tuned load upon which the gain is dependant. For a parallel resonating circuit consisting of a capacitor, C and an inductor L the impedance Z_o is maximum at resonant frequency, $f_o = 1/(2\pi\sqrt{LC})$. So an amplifier with tuned load will have maximum gain at resonant frequency. In practical tuned amplifier circuits, an intermediate frequency transformer (IFT) is used as tuned load. IFT is tuned to standard 455 kHz audio frequency. The quality factor of the circuit is given by Q = fo/ Bandwidth.

CIRCUIT DIAGRAM:



DESIGN:

In order to design a common emitter amplifier operating at high frequency, one can use a high frequency transistor like BF194, BF195, BF494, BF495 or 2N2222.

Let V_{CC} be 10% more than the required output amplitude.

Ic < 10% of I_{Cmax}

Assume suitable values for Ic and the stability factor of the circuit be S.

Under dc conditions, the primary dc resistance of the IFT is very small (< 5Ω). So dc voltage drop across collector circuit is very low, approximately zero.

For class A mode of operation set,

$V_{CE} = V_{CC}/ 2$

Design of Emitter resistance:

The voltage across emitter resistance is, $V_{RE} = V_{CC} - V_{CE}$

$I_E \approx I_C$.

Thus $R_E = V_{RE} / I_E$

Choose standard value of R_E.

Design of Potential divider biasing:

Let the Stability factor be S

Assuming R_B is the effective resistance at the base,

$S = 1 + R_B/ R_E$

$R_B = 9R_E$

$R_B = R_1||R_2 = R_1R_2/(R_1 + R_2)$

The voltage at the base of the transistor is

$V_B = V_E + V_{BE} = V_{RE} + V_{BE}$.

This is the voltage across R1.

$V_{R1} = V_{CC}R_2/(R_1 + R_2)$

$R_2/(R_1 + R_2) = V_{R1}/V_{CC}$

Thus, values of R_1 and R_2 can be determined.

Choose appropriate value for load resistor, R_L

Design of capacitors:

The capacitors C_1, C_2 and C_E can be designed based on lower cut-off frequency at -3 dB point. Since this frequency is much lower than 300 kHz, Choose low values of capacitance like $C_1 = C_2 = C_E$.

PROCEDURE:

1. Assemble the circuit as shown in the circuit diagram.
2. Obtain output from output-1 or output-2 terminal as in the circuit diagram.
3. Give input signal, which is a sinewave of frequency which is variable of appropriate amplitude.
4. Observe the output waveform on a CRO.
5. Enter the details of input and output waveforms on the tabular column shown.
6. Calculate gain A_V by varying f_{in}.(A_V = Voutpp/ Vinpp)
7. Plot frequency response characteristics with f_{in}(kHz) along x-axis and Gain(dB) = 20 log A_V along y-axis.
8. Find the resonant frequency, 3-dB bandwidth and hence the Q-factor.

5. FM USING 555 IC

AIM: To design and set up a frequency modulating circuit using 555.

COMPONENTS AND EQUIPMENT REQUIRED:

555 Timer IC, resistors, capacitors, signal generator, power supply and DSO.

THEORY:

Frequency modulation is an analog modulation technique in which the frequency of the carrier is varied in accordance with the message signal amplitude.

Modulation index for FM is

m =δf/fm = frequency deviation/modulating signal frequency.

555 is an IC which can be used to set up an astable multivibrator of 50% duty cycle whose frequency is determined by externally connected RC load. The standard design equation for an astable multivibrator using 555 timer IC is defined by the following equation for its time period.

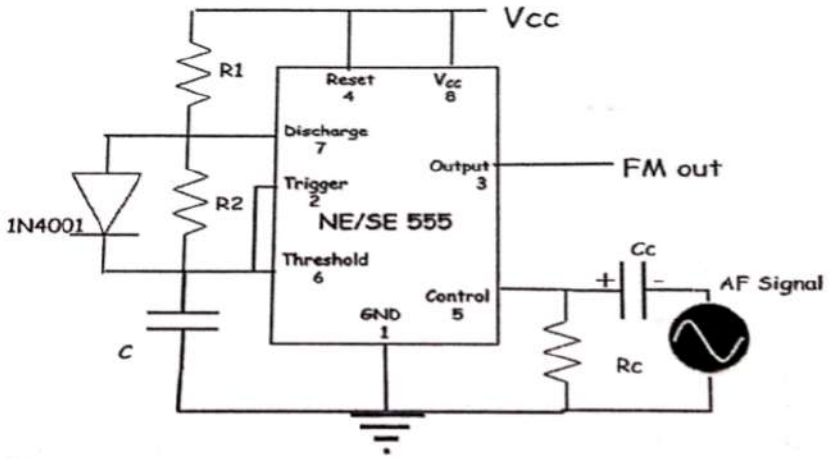
$$T = 1.38RC$$

Thus its frequency of oscillation is:

$$f_0 = \frac{0.72}{RC}$$

This frequency of oscillation remains constant as long as the pin-5 is supplied with a constant voltage. If the voltage at pin-5 is varying the frequency of oscillation of the astable multivibrator also changes along with it. Thus a stable multivibrator using 555 can be used as a carrier pulse generator. The frequency of the carrier can be varied by feeding the pin-5 with message signal.

CIRCUIT DIAGRAM:



DESIGN:

Take appropriate values of V_{CC} and $f_{free\text{-}running}$ = f_{center} frequencies.

$\therefore T_{charging} = T_{discharging} = \frac{1}{2 f_{center}}$

But, $T_{charging} = T_{discharging} = \ln(2RC)$

Take appropriate values of C.

Then, $R_1 = R_2 = \frac{T_{charging}}{\ln(2 * C)}$

Take suitable values for R_c and C_c for AC coupling.

PROCEDURE:

1. Set up the circuit and observe the function of 555 IC as AMV.
2. Apply modulating signal and observe the FM output.

6. FM GENERATION AND DEMODULATION USING PLL

AIM: To design and setup a frequency modulator and demodulator circuit using CMOS PLL IC 4046.

COMPONENTS AND EQUIPMENTS REQUIRED:

PLL IC 4046, Resistors, Capacitors, Op-amp IC 741, DC Power supply, function generator and DSO.

THEORY:

CD 4046 is an analog Phase Locked Loop IC which can be used for FM modulation and demodulation.

FM Modulation

The VCO part of the PLL may be used for the frequency modulation of the carrier. In a VCO, the output frequency is proportional to the control voltage input. In the absence of control voltage, the free running frequency is determined by the supply voltage V_{CC}, the externally connected resistances R_1 and R_2 and the capacitance C. The free running frequency f_0 is given by:

$$f_0 = \frac{0.16 Vcc/2}{R_1 C} + \frac{1}{R_2 C}$$

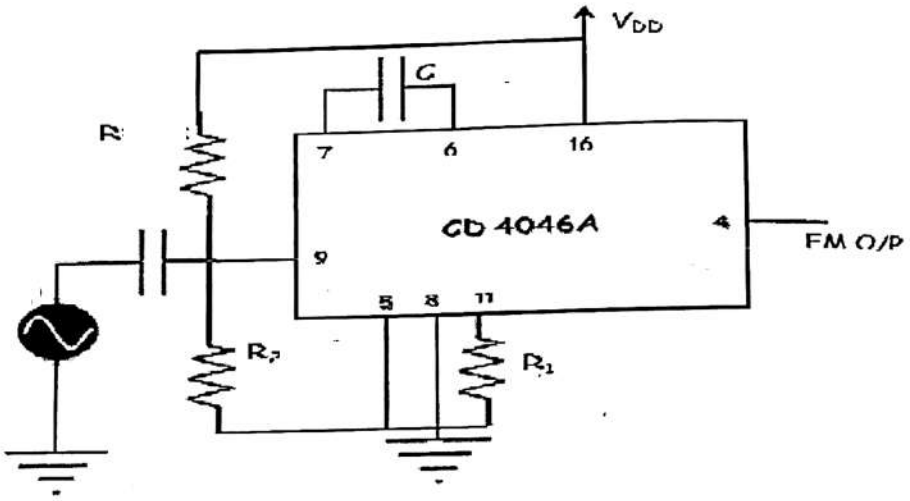
The VCO in free running mode is the carrier generator. The carrier frequency is f_0. The control input of the VCO is clamped at a voltage Vcc/2. The modulating signal voltage which is less than Vcc/2 is applied at this pin through a capacitor. This results in variation in the frequency of oscillation of the VCO, which is the frequency modulated signal.

FM Demodulation:

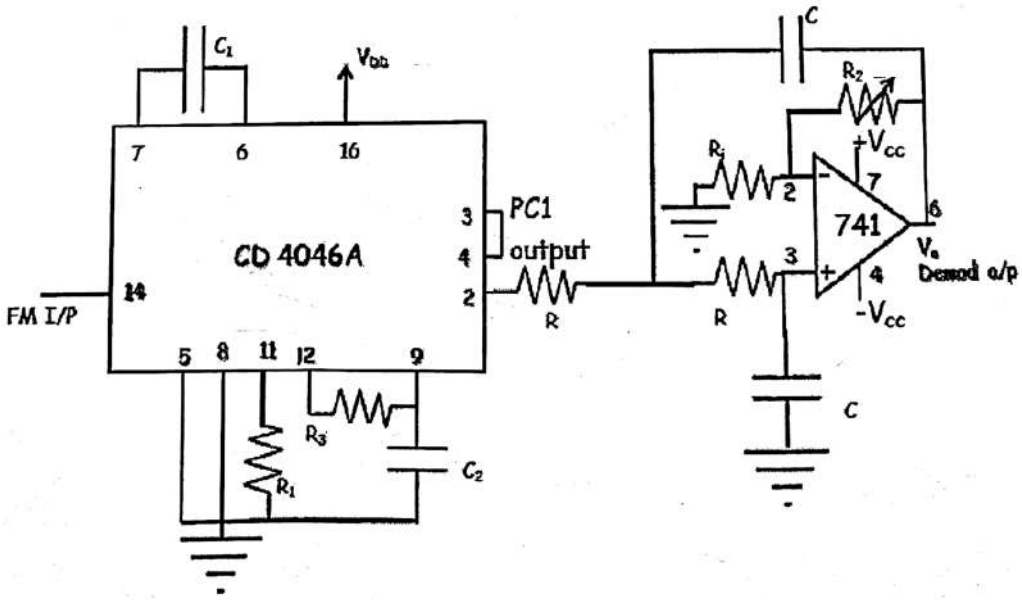
Another PLL IC has to be used for FM demodulation. The VCO part of this IC is configured for the same free running frequency as that of the modulator IC. One of the phase detector input is fed with the modulated FM signal and the other input of the phase detector is fed with the VCO output after filtering out high frequency components. The phase variation between the two will be corresponding to the message which was used for modulation. The phase detector output is passed through an emitter follower internally to the demodulated output pin. The output from this pin may contain high frequency ripples which may be eliminated by proper filtering to obtain the actual message.

CIRCUIT DIAGRAM:

FM GENERATION USING CMOS PLL IC:



FM DEMODULATION USING CMOS PLL IC & ACTIVE 2nd ORDER LPF:



DESIGN:

VCO centre frequency $f_0 = \frac{2R_1}{1/¿}$ (C_1 +32pF))

Select appropriate values of C_1 and f_0, then

$R_1=1/(2 \times f_0 \times (C_1 +32pF))$

With general assumptions of lock range, $2\Delta f_L$ and capture range $2\Delta fc$ frequencies,

$2\Delta f_c=2\sqrt{(f_1\Delta f_1)}$

$\Delta fc^2=\Delta f_L/(2\Pi R_3 C_2)$

Assume suitable value of C_2

Then $R_3 = \Delta f_L/(2\pi C_2 \Delta fc^2)$

For active second order filter, the cut-off frequency is given by

$$f = \frac{1}{2\pi RC}$$

Take general values of C and f,

$$R = \frac{1}{2\pi fC}$$

For Butterworth LPF,

$1+R_2/R_1 = A$

For suitable values of R_1 find R_2.

PROCEDURE:

1. Set the FM generator circuit and feed sine wave input and observe FM output at pin number 4.
2. Set up the demodulator and feed the FM signal to it. The PC1 output (output of XOR gate) will be a PWM output.
3. PC1 output at pin 2 is fed to active second order Sallen -Key LPF and observe the demodulated output.

7. FREQUENCY MULTIPLIER USING PLL

AIM: To design and set up a frequency multiplier using CD4046 PLL IC to multiply an input frequency by a factor N.

COMPONENTS AND EQUIPMENTS REQUIRED:

CD4046A PLL IC, IC 7490, Resistors, Capacitors, DC power supply, Function generator and DSO.

THEORY:

The output from the PLL system can be obtained either as the voltage signal V(t) corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application, whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

In the case of a frequency output, the input signal is comprised of many frequency components corrupted with noise and other disturbances. The PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency and attenuate other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal out of many undesirable frequency signals.

The counter IC 7490

This asynchronous TTL MSI decade counter has a mod-2 counter and mod-5 counter inside it, if the clock is applied at input B, mod-5 counter output will appear at Q3Q2Q1. If the clock is applied at input A, Q0 is connected to input B, we get binary decade output from Q3Q2Q1Q0. A logic 1 level at reset input R(1) and R(2) will make all the flip flops reset. A high level at both Set input S(1) and S(2) will set the counter output ‘1001’.

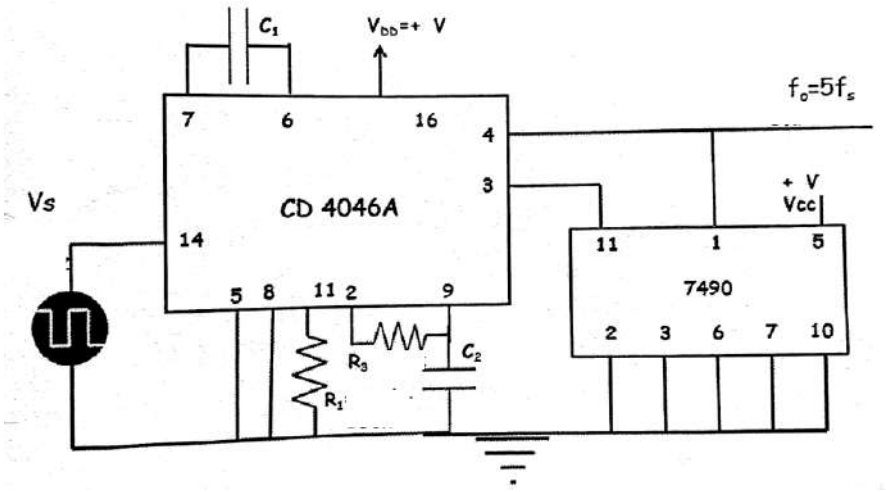
Frequency Multiplication

A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency is given by,

$$f_0 = N f_s$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter. Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the signal is rich in harmonics, i.e., square wave, pulse train etc, then VCO can be directly locked to the n^{th} harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n, typically n is kept less than 10.

CIRCUIT DIAGRAM:



DESIGN:

VCO centre frequency $f_0 = \frac{2R_1}{1/¿}$ (C_1 +32pF))

Assume suitable values for C_1 and f_0, then

$R_1 = \frac{2f_0}{1/¿}$ (C_1 +32pF)) (Use std.values)

With general assumptions of lock range, $2\Delta f_L$ and capture range $2\Delta fc$ frequencies,

$2\Delta f_c = 2\sqrt{(f_1 \Delta f_1)}$

$\Delta fc^2 = \Delta f_L/(2\Pi R_3 C_2)$

Assume suitable value for C_2

Then find $R_3 = \Delta f_L/(2\pi C_2 \Delta fc^2)$

PROCEDURE:

1. Set up the circuit stage by stage, verify the working of PLL and counter separately.
2. Complete the circuit and apply square wave at the input and observe the multiplied frequency.

8. PRE-EMPHASIS AND DE-EMPHASIS CIRCUITS

AIM: To study and test the characteristics of pre-emphasis and de-emphasis circuits.

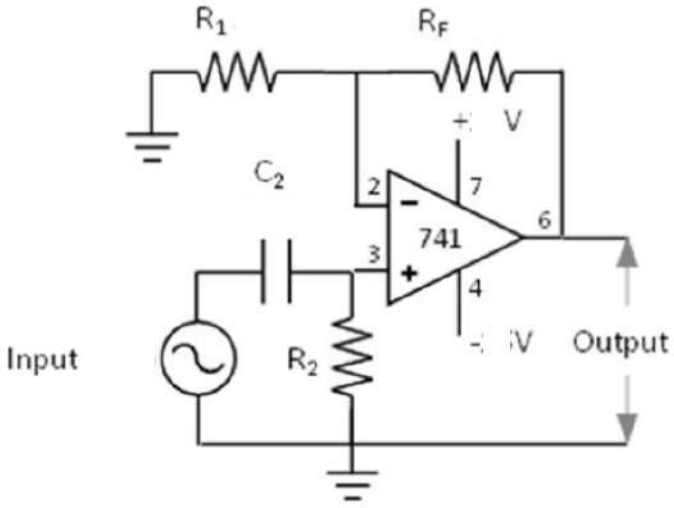
COMPONENTS AND EQUIPMENT REQUIRED:

IC 741, Resistors, Capacitor, Signal Generator, CRO, Power Supply, Breadboard.

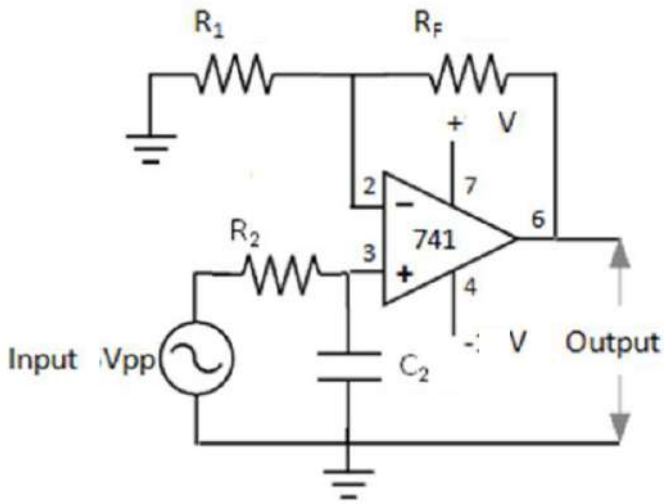
THEORY:

In FM Broadcasting, the effect of noise is more intense on higher frequencies than on low frequencies. Therefore, in order to have high signal-to-noise ratio (low noise), the high frequencies are amplified at the transmitter side (pre-emphasis) and for compensation, de-emphasis (decreasing the amplitude of those boosted frequencies) is done at receiver. The pre-emphasis circuit is actually a high pass filter and de-emphasis circuit a low pass filter. The amount of pre-emphasis and de-emphasis used is defined by the time constant of a simple RC filter circuit. Simple pre-emphasis and de-emphasis circuits using op-amp are given in the diagram.

CIRCUIT DIAGRAM:



Pre-emphasis Circuit



De-emphasis circuit

DESIGN:

Choose appropriate value for Time constant, T

Therefore, the time constant T = RC

With general assumptions of value of C, then find R = T / C

For Butterworth filters, Gain A = 1.586

Gain of non-inverting amplifier = $1+R_f/R_1$

$1.586 = 1+R_f/R_1$

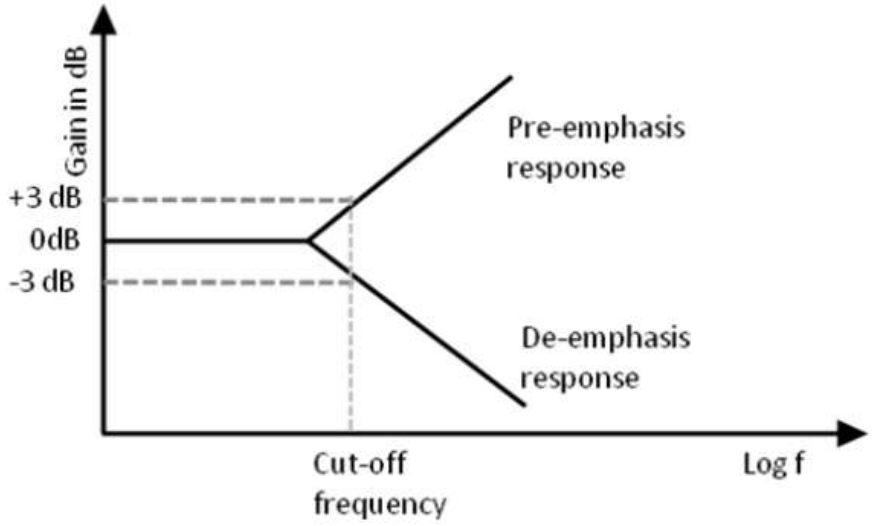
$R_f/R_1 = 0.586$

Take suitable value of R_1, then find R_f.

PROCEDURE:

1. Test all the components and probes.
2. Set up the pre- emphasis circuit on a bread board as shown in figure.
3. Feed a sine wave as input. Vary the frequency from few Hz to few MHz and note down the values of the corresponding output voltage on a tabular column.
4. Plot frequency response on a graph sheet with log f on x-axis and gain in dB on y-axis.
5. Mark the cut-off frequencies corresponding to 3dB points.
6. Repeat the above steps for de-emphasis circuit.

FREQUENCY RESPONSE:



9. ANALOG SIGNAL SAMPLING AND RECONSTRUCTION

AIM: To set up sampling and reconstruction circuits to study the sampling theorem and to plot waveforms for different sampling rates.

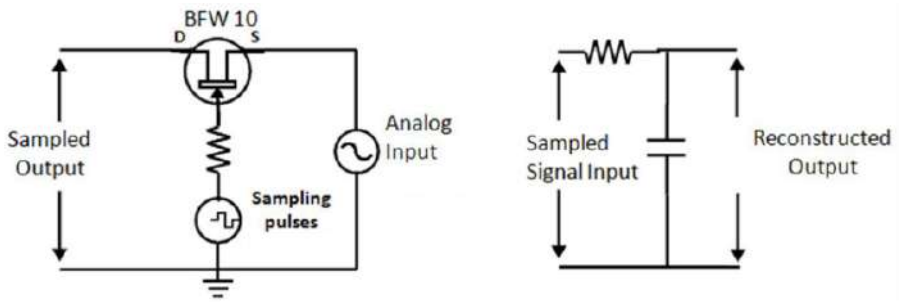
COMPONENTS AND EQUIPMENT REQUIRED:

FET BFW 10, Resistors, Capacitor, Signal Generator, CRO, Bread Board, Wires and probes.

THEORY:

As a first step to convert analog signals into digital form, the samples of the analog signals are taken at regular intervals. The levels of these samples are then encoded and send to the receiver. At the receiver these samples are recovered and from that the original signal is reconstructed. Sampling theorem states that the original signal can be faithfully reconstructed only if the sampling frequency is at least double that of the highest frequency component in the sampled signal. A sampling and reconstruction circuit is shown in figure. An FET is used as a switch to take samples of the sine wave input. Sampling pulses are applied to the gate of the FET that switches it ON and OFF. The input signal is sent to the output only when the transistor is ON. Thus, the output of the FET is a sampled form of the input signal. The reconstruction circuit is a low pass filter having a cut off frequency equal to the frequency of the analog input signal.

CIRCUIT DIAGRAM:

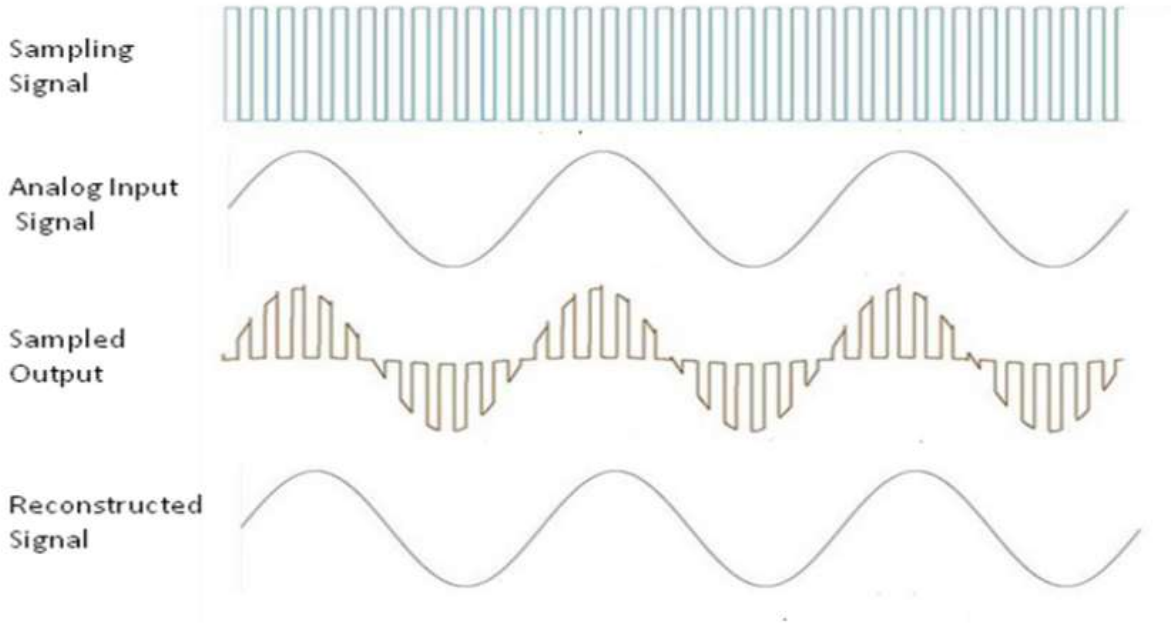


PROCEDURE:

1. Test all the components and probes.
2. Set up the circuit as shown in figure on the bread board.

3. Feed a sine wave as input.
4. Apply a square wave signal as sampling pulse
5. Observe sampled output and reconstructed signals for different sampling frequencies.
6. Vary the amplitude of the sampling pulses to obtain the optimum output.
7. Plot the above waveforms.

WAVEFORMS



10. GENERATION OF PSEUDO-NOISE BINARY SEQUENCE USING SHIFT REGISTERS

AIM:

To set up a linear feedback shift register (LFSR) and to design it as a Pseudo-Random Binary Sequence (PRBS) generator.

COMPONENTS AND EQUIPMENTS REQUIRED:

Digital IC 7474, 7486, Digital IC trainer kit, function generator and DSO.

THEORY:

PRBS is stands for Pseudo-random binary sequence; it can be useful in many applications.

Pseudo random binary sequences (PRBS) show up in many applications such as cryptography and communications, but my main interest in them stems for their use in providing pseudo random data for generating eye pattern diagrams (EPD).

A shift register and a XOR gate are used to construct a PRBS generator and is useful to generate the PRBS waveform.

The inputs to the feedback network (input to the XOR gate is given from any two flip-flop output and output of XOR is given to the input of shift register), which have to be linear and follow combinational logic, are the outputs at selected stages of the shift register.

The maximum length of the PRBS waveform is (2" - 1) bits, where n is the number of stages in the shift register.

It can be obtained by a proper choice of the tappings for the shift register. The tappings have been mathematically evaluated and published in tabular form.

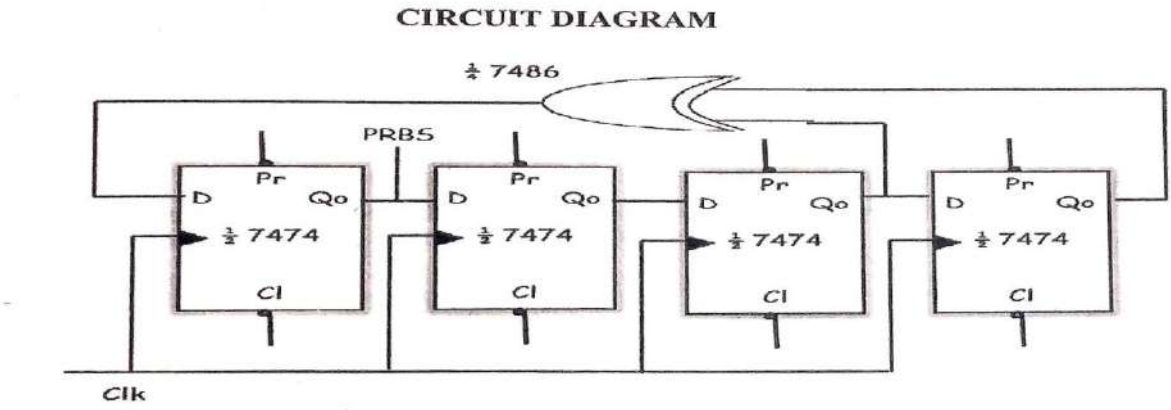
The frequency of the PRBS waveform is the same as the clock frequency of the shift register.

The initial value of the LFSR is called the ’seed’ and because the operation of the register is deterministic; the sequence of bits produced by the register is completely determined by the current state. LFSR has a well-chosen feedback function and produces a sequence of bits which appear random having a long cycle. The sequence repeats after every (2" - 1) cycles. PRBS signals are used in spread spectrum communication applications.

SAMPLE SEQUENCE:

0001,1000,0100,0010,1001,1100,0110,1011,0101,1010,1101,1110,1111,0111,0011,0001
0110,1011,0101,1010,1101,1110,1111,0111,0011,0001,1000,0100,0010,1001,1100,0110
1010,1101,1110,1111,0111,0011,0001,1000,0100,0010,1001,1100,0110,1011,0101,1010

CIRCUIT DIAGRAM:



PROCEDURE:

1. Set up the circuit and clear the flip-flops using clear-pins.
2. Using the preset pin, preset the flip-flops randomly.
3. Feed clock pulses and observe the PRBS outputs from Q_0 and verify that PRBS repeats after every (2" - 1) cycles.

11. TIME DIVISION MULTIPLEXING & DEMULTIPLEXING

AIM:

To set up Time Division Multiplexer and Demultiplexer circuits and to observe the waveforms.

COMPONENTS ADN EQUIPMENT REQUIRED:

Transistor- SL100, SK100, resistors, capacitors, Op-amp, signal generator, power supply, DSO.

THEORY:

Time Division Multiplexing (TDM) is widely used in digital communication networks to transmit multiple signals simultaneously through the same channel. Different signals are transmitted in a time shared manner. Each signal is allotted a fixed time slot and a sample of the corresponding signal is transmitted during that period. After one sample each of all the signals is sent, the time slot is given back to the first signal and this process repeats.

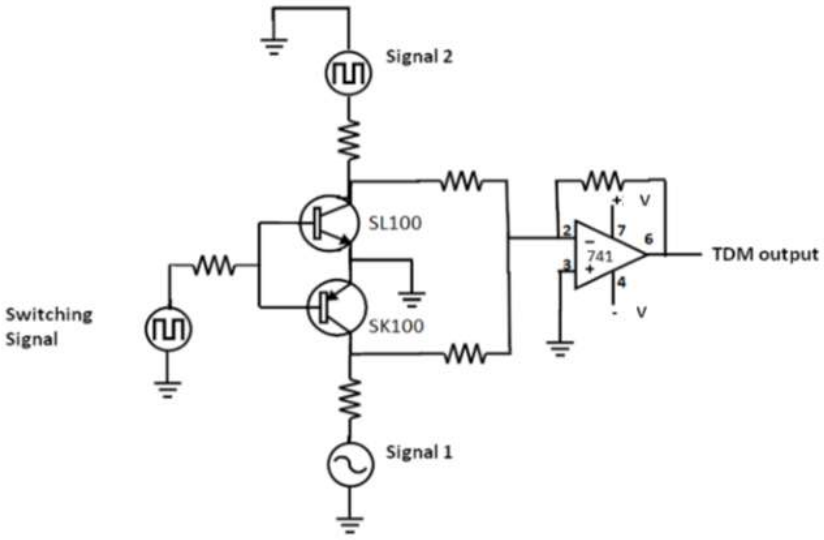
TDM Multiplexer

A simple TDM multiplexer circuit using an NPN-PNP transistor pair and an Op amp is shown in figure. The transistors work as switches and the Op amp works as an adder. The signals to be sent are fed to the collectors of the two transistors. The switching signal is applied to the bases the transistors. During the ON time of the switching signal, the NPN transistor is ON and the PNP transistor is OFF. Signal 1 alone is connected to the adder input and reaches the output. During OFF time of the switching signal, the NPN transistor is OFF and the PNP transistor is ON. Signal 2 alone is connected to the adder input and reaches the output. Thus the two signals reach the output one after the other as the switching signal changes state. The resulting signal is a time division multiplexed one. The on-off period of the switching signal decides the time slot.

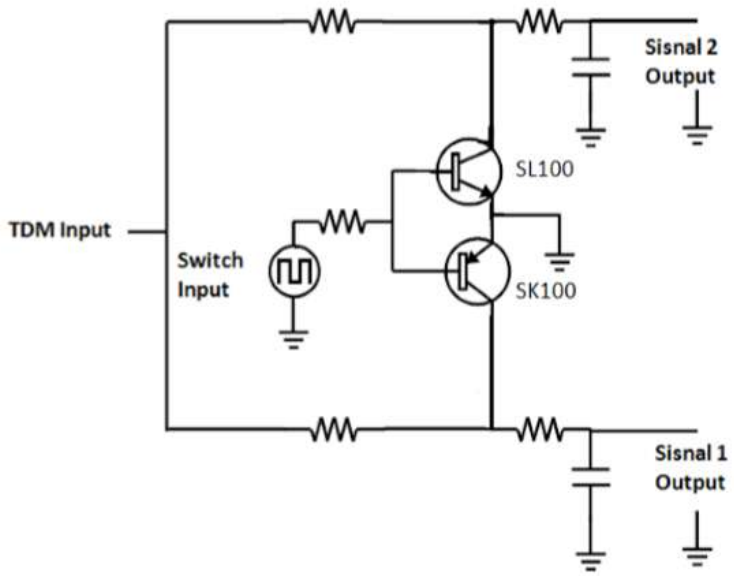
TDM Demultiplexer

In the demodulator circuit the two transistors act as switches. They connect the input TDM signal to the respective outputs alternately as the switching signal changes state. A square wave signal with the same phase and frequency as the one used at the TDM modulator is used as the switching signal. During the ON time of the switching signal, the NPN transistor is ON and the PNP transistor is OFF. TDM input is now connected to signal 1 output. During the OFF time of the switching signal, the NPN transistor is OFF and the PNP transistor is ON. TDM input is now connected to signal 2 outputs. The RC networks act as low pass filters.

CIRCUIT DIAGRAM:

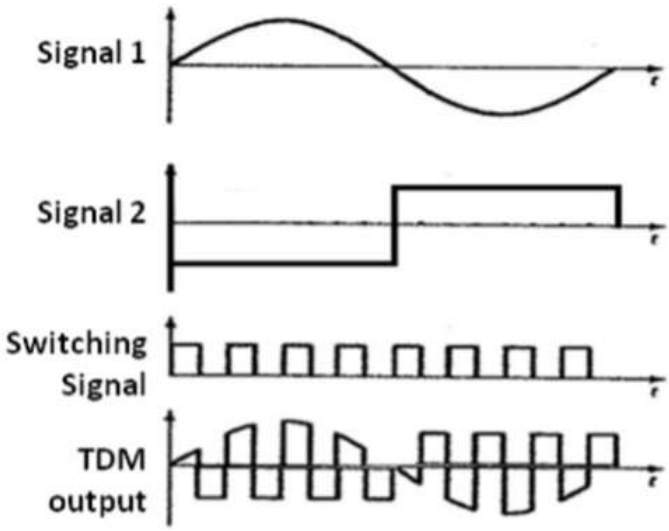


TDM Multiplexer



TDM Demultiplexer

SAMPLE WAVEFORM:



PROCEDURE:

1. Test all the components and probes.
2. Set up the circuits on the bread board as shown in figure.
3. Connect a square wave signal as the switching input.
4. Connect a sine wave as signal 1 and a square wave as signal 2.
5. Observe the TDM output on CRO and plot the waveforms.
6. Feed this TDM output to the input of the de-multiplexer. Use the same square wave signal used at the modulator as the switching signal.
7. Observe signal 1 and signal 2 outputs of the de-multiplexer on CRO.
8. Plot the waveforms.

12. GENERATION AND DETECTION OF DM/SIGMA-DELTA/ADM

(A) DELTA MODULATION

AIM: To design, set up and study a Delta Modulator

COMPONENTS AND EQUIPMENTS REQUIRED:

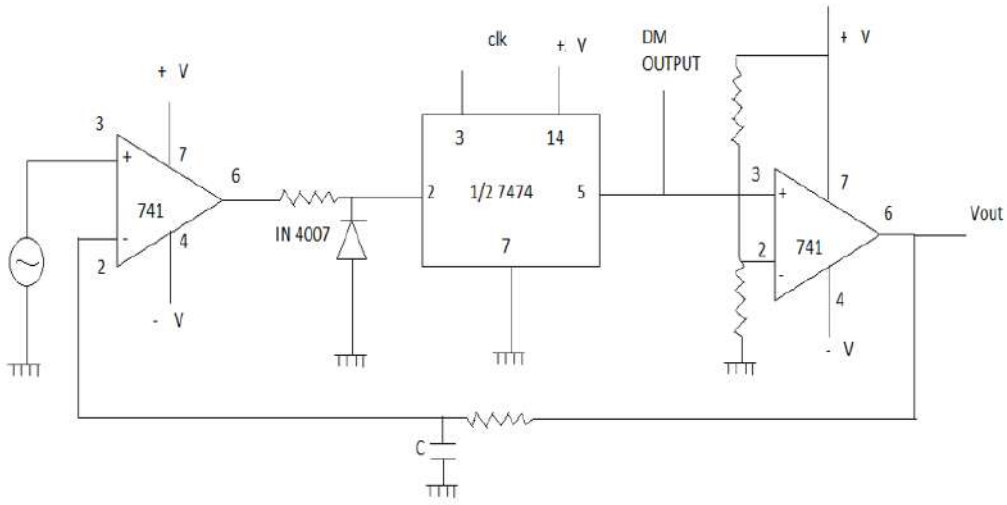
OP-amp, 7474 IC, resistors, capacitors, signal generator, DC supplies, bread board and CRO.

THEORY:

Delta modulation is a differential PCM scheme in which the difference signal is encoded into a single bit. This single bit is transmitted per sample to indicate whether the signal is larger or smaller than the previous sample. Circuit for delta modulation is shown in the figure. The modulating signal m(t) and its quantized approximation $\hat{m}$ (t) are applied to the comparator. Comparator provides a high level output when m(t) < $\hat{m}$ (t).

The output of the input comparator is fed to a sample and hold circuit made by a D flip-flop. The clock frequency to flip-flop is selected at sampling rate. Pulses at the output of D flip-flop are made bipolar by an op-amp comparator. Bipolar pulses are converted to analog signal before feeding to the comparator using an RC low pass filter.

CIRCUIT DIAGRAM:



DESIGN:

Assume a clock frequency.

Integrator:

$R_4C_1 > 16T$, $T = \frac{1}{clock\ frequency}$

Assume a suitable value for C1, then calculate R_4.

Comparator:

With general assumptions of V_{CC} and R3

Design R2 such that voltage at terminal 2 is V

(any V such that 0<V<5)

Therefore $\frac{VCC \times R3}{R2+R3} = V$

And Hence, calculate R3.

PROCEDURE:

1. Set up the circuit after verifying the conditions and components
2. Feed a unipolar sine wave to the input using offset knob of function generator. Set an appropriate clock frequency.
3. Observe the DM output and V_o simultaneously on CRO screen.

(B) DELTA-SIGMA MODULATION

AIM:

To realise a circuit to produce delta-sigma modulation and observe the waveforms.

COMPONENTS AND EQUIPMENT REQUIRED:

IC 7474, IC 741, resistors, capacitors, power supply, signal generator.

THEORY:

Delta-sigma (ΔΣ; or sigma-delta, ΣΔ) modulation is a method for encoding analog signals into digital signals as found in an analog-to-digital converter (ADC). It is also used to convert high bit-count, low-frequency digital signals into lower bit-count, higher-frequency digital signals as part of the process to convert digital signals into analog as part of a digital-to-analog converter (DAC).

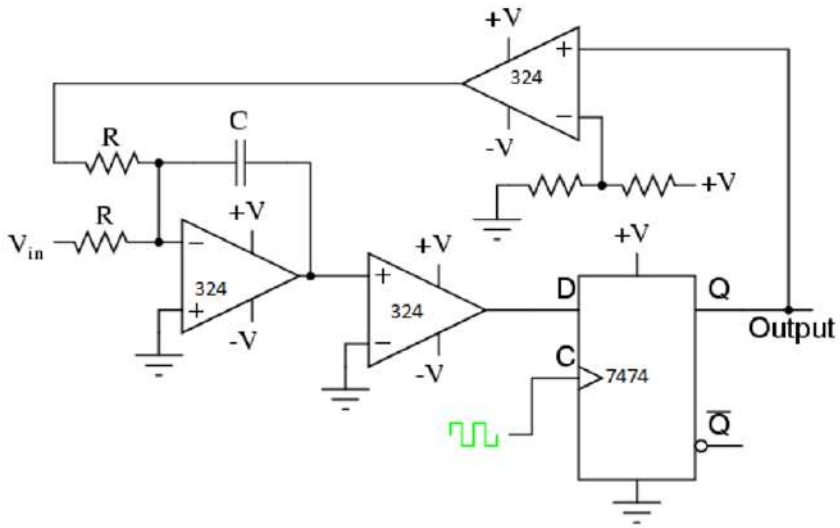
In a conventional ADC, an analog signal is sampled with a sampling frequency and subsequently quantized in a multi-level quantizer into a digital signal. This process introduces quantization error noise. The first step in a delta-sigma modulation is delta modulation. In delta modulation the change in the signal (its delta) is encoded, rather than the absolute value. The result is a stream of pulses, as opposed to a stream of numbers as is the case with pulse code modulation (PCM). In delta-sigma modulation, accuracy of the modulation is improved by passing the digital output through a 1-bit DAC and adding (sigma) the resulting analog signal to the input signal (the signal before delta modulation), thereby reducing the error introduced by the delta modulation.

Both ADCs and DACs can employ delta-sigma modulation. A delta-sigma ADC first encodes an analog signal using high-frequency delta-sigma modulation, and then applies a digital filter to form a higher-resolution but lower sample-frequency digital output. A delta-sigma DAC encodes a high-resolution digital input signal into a lower-resolution but higher sample-frequency signal that is mapped to voltages, and then smoothed with an analog filter. In both cases, the temporary use of a lower-resolution signal simplifies circuit design and improves efficiency.

Primarily because of its cost efficiency and reduced circuit complexity, this technique has found increasing use in modern electronic components such as DACs, ADCs, frequency synthesizers, switched-mode power supplies and motor controllers. The coarsely-quantized

output of a delta-sigma modulator is occasionally used directly in signal processing or as a representation for signal storage.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Assemble the circuit on bread board.
2. Firstly, the output of the integrator should be a waveform closely following the input waveforms.
3. Observe the results in a serial stream of output bits by the flip-flop. If the analog input is 0V, the integrator will have no tendency to ramp either positive or negative, except in response to the feedback voltage.

(C) ADAPTIVE DELTA MODULATION

AIM: To study the characteristics of adaptive delta modulation and demodulation kit.

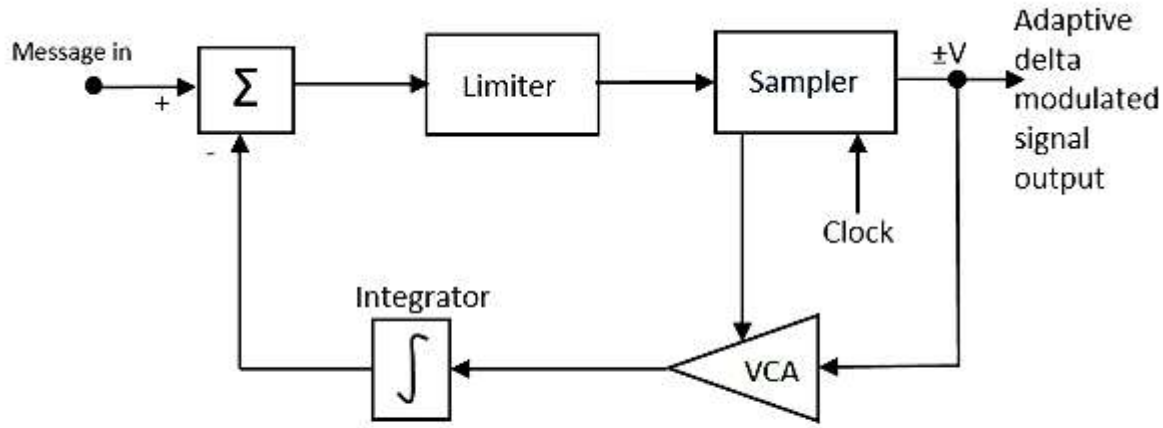
COMPONENTS AND EQUIPMENT REQUIRED:

Delta modulation and demodulation Kit, Digital Storage Oscilloscope (DSO), Power supply, Patch cords

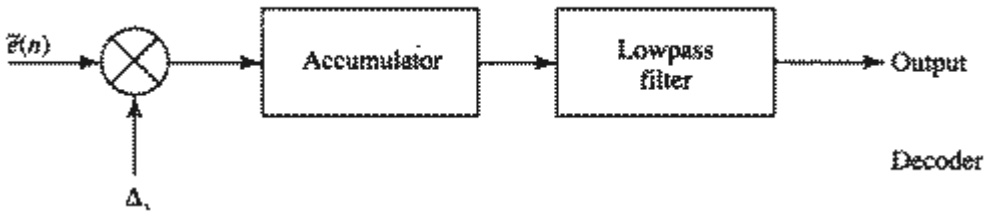
THEORY:

A large step size was required when sampling those parts of the input waveform of steep slope. But a large step size worsened the granularity of the sampled signal when the waveform being sampled was changing slowly. A small step size is preferred in regions where the message has a small slope. This suggests the need for a controllable step size - the control being sensitive to the slope of the sampled signal. The gain of the amplifier is adjusted in response to a control voltage from the sampler, which signals the onset of slope overload. The step size is proportional to the amplifier gain.

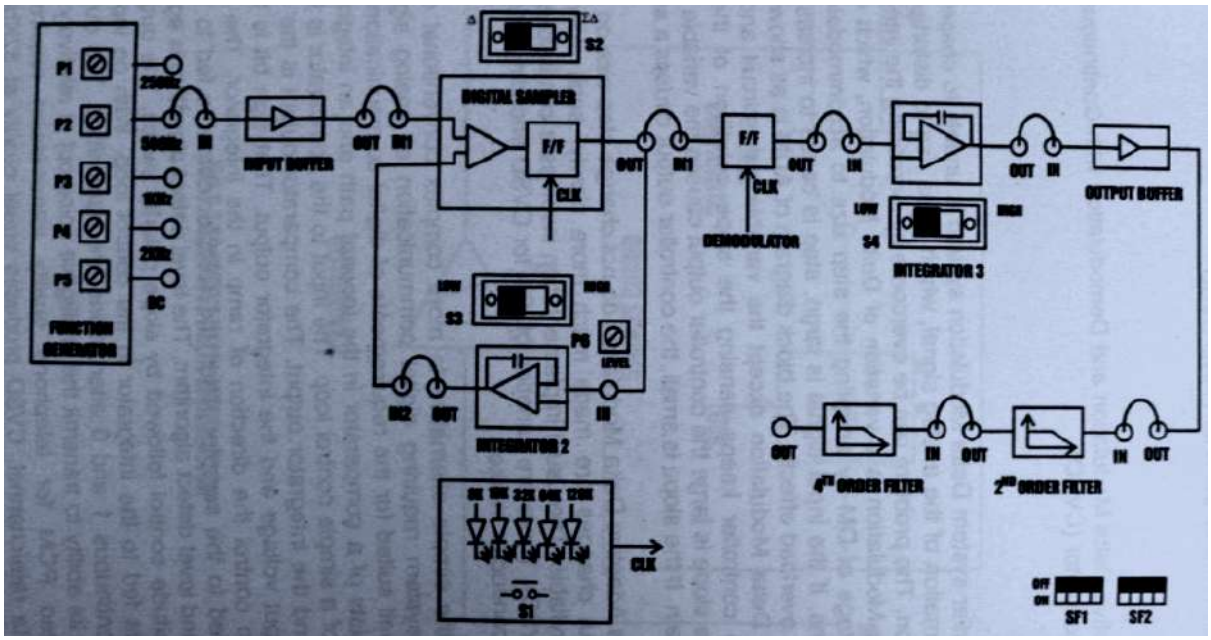
CIRCUIT DIAGRAM:



Adaptive delta modulator



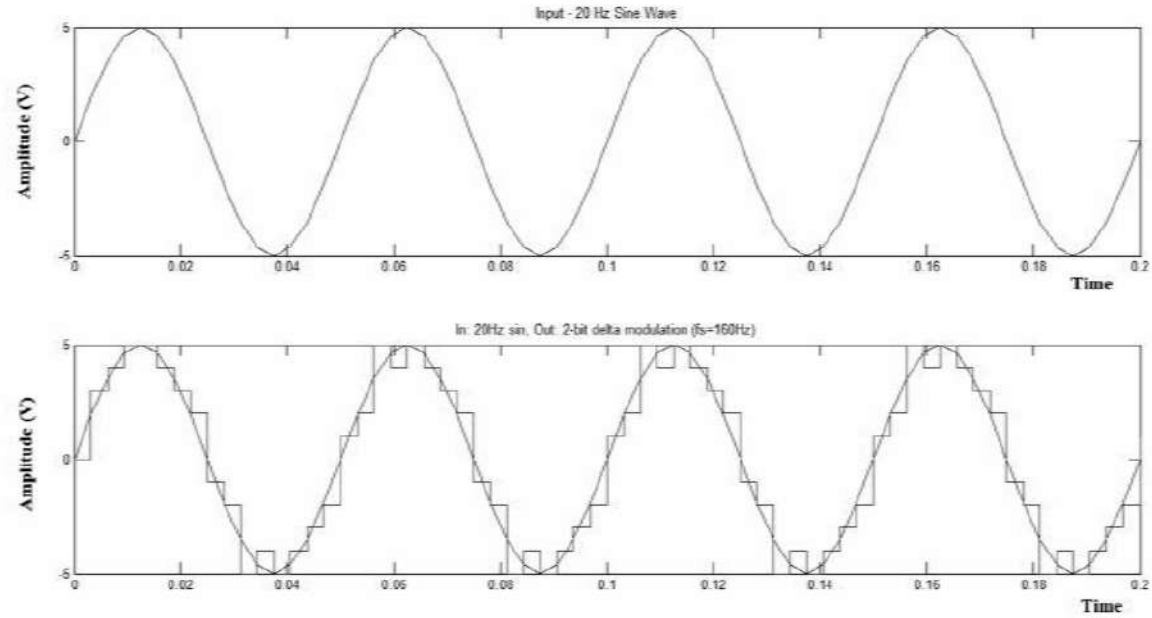
Demodulator



PROCEDURE:

1. The connections are given as per the block diagram.
2. Connect power supply in proper polarity to kits DCL-07 and switch it on.
3. Keep the Switch S2 in sigma delta position.
4. Keep the Switch S3 High.
5. Observe the various tests points in demodulator section and observe the reconstructed signal through 2nd order and 4th order filter.

MODEL GRAPH


Input - 20 Hz Sine Wave
Amplitude (V)
Time
In: 20Hz sin, Out: 2-bit delta modulation (fs=160Hz)
Amplitude (V)
Time

13. GENERATION AND DETECTION OF PAM/PWM/PPM

(A) PAM

AIM: To set up pulse amplitude modulator and demodulator circuits and to observe the waveforms.

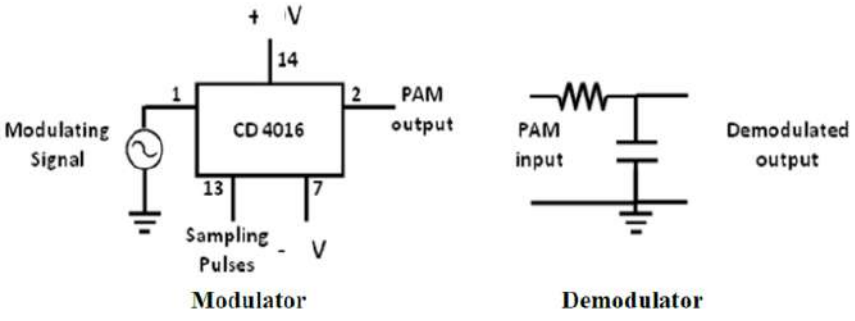
COMPONENTS AND EQUIPMENT REQUIRED:

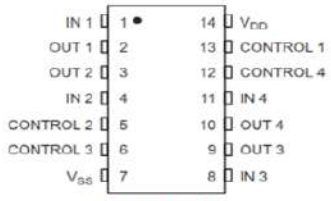
Analog Switch CD 4016, Resistor, Capacitor, Signal Generator, CRO, Breadboard, Power supply

THEORY:

Pulse Amplitude Modulation (PAM) is the simplest pulse modulation scheme. In pulse amplitude modulation system the amplitude of a carrier pulse train is varied in accordance with the instantaneous level of the modulating signal. The simplest form of the PAM modulator is an analog switch that is turned on and off at the RF carrier pulse rate. As the switch changes state, the modulating signal is connected and disconnected from the output. Thus the output PAM signal is a sampled version of the modulating signal. If the sampling frequency is sufficiently high (at least twice that of the highest modulating frequency), the original signal can be recovered at the receiver by simply passing it through a low pass filter having a cut-off frequency equal to the highest frequency in the modulating signal.

CIRCUIT DIAGRAM:





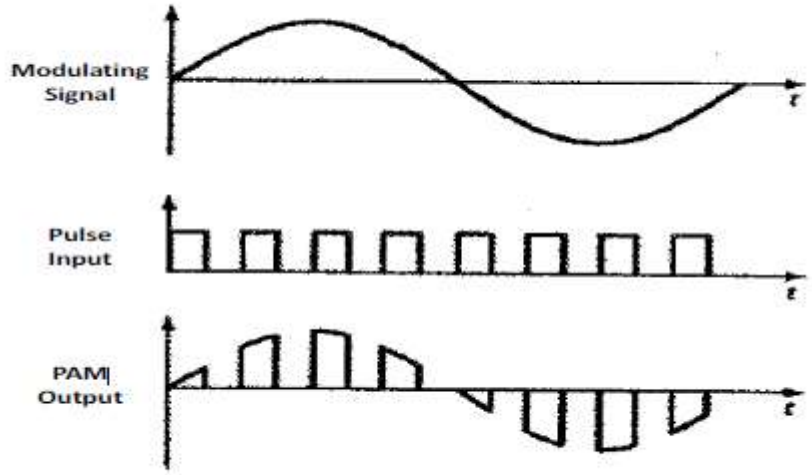
CD 4016 Pinout

PROCEDURE:

1. Test all the components and probes.

2. Set up the modulator circuit using CD 4016 as shown in figure.
   Switch on the power supplies.
3. Feed a modulating signal at IN 1 input and square wave signal at control 1 input of CD 4016.
4. Observe the PAM output signal at OUT 1 pin on one channel of the CRO.
5. Set up the demodulator circuit as shown in figure. Feed the PAM signal as the input and observe the demodulated output on the other channel of the CRO. Plot the waveforms.

WAVEFORM:



(B) PWM

AIM: To set up pulse width modulator and demodulator circuits and to observe and plot the waveforms.

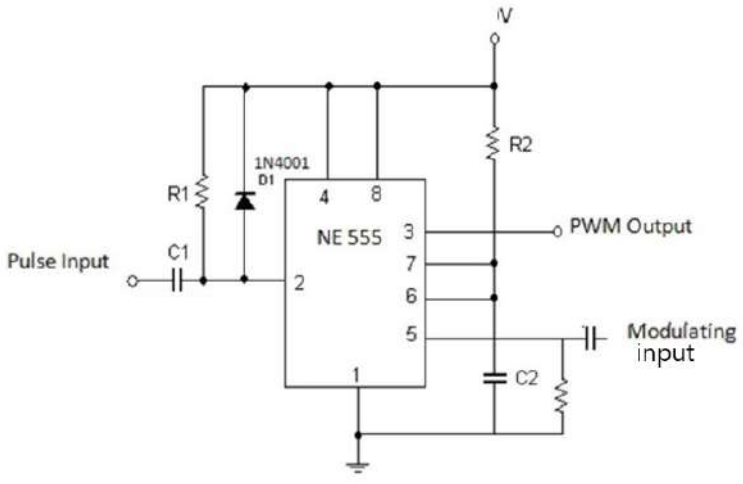
COMPONENTS AND EQUIPMENTS REQUIRED:

IC 555, IC 741, Resistors, Capacitors, Diode 1N 4001, CRO , Signal Generator, Bread Board, Power Supply, Wires and connectors.

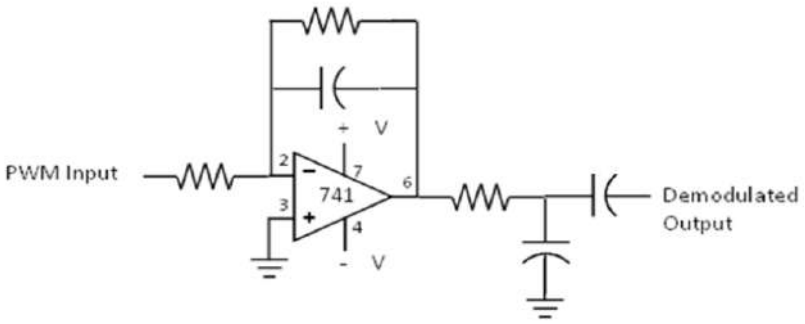
THEORY:

Pulse Width Modulation (PWM) is a form of pulse modulation where the width of the pulses in a carrier pulse train is made proportional to the instantaneous amplitude of the modulating signal. A pulse width modulator circuit made up of 555 Timer is shown in figure. Here the 555 timer is working in monostable mode. A negative trigger pulse at pin 2 sets the output. The modulating signal is applied to the control pin of the 555 which varies the threshold voltage. This in turn varies the charging time of capacitor C_2 and makes the trailing edge of the output pulse proportional to the modulating signal. Thus the leading edge of the output pulse is decided by the trigger pulse which occurs periodically and the trailing edge is proportional to the amplitude of the modulating signal. The resulting output will be pulse width modulated. The pulse width demodulator circuit consists of an integrator and a low pass filter with a cut off frequency of 100Hz. The integrator reconstructs the modulating signal which is further smoothened by the low pass filter. The series capacitor eliminates the dc component from the demodulated signal.

CIRCUIT DIAGRAM:



Modulator

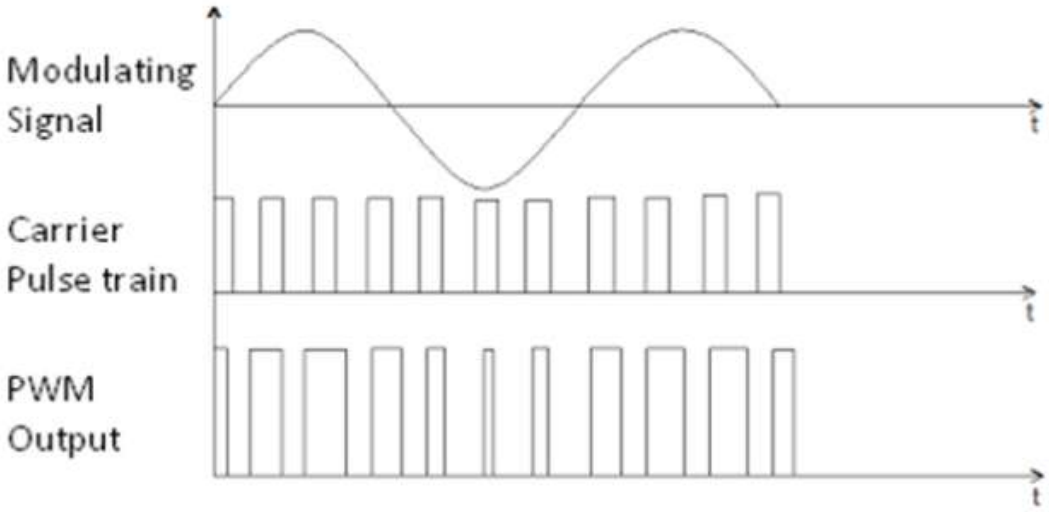


Demodulator

PROCEDURE:

1. Test all the components and probes.
2. Set up the circuit as shown in the figure on the bread board. Switch on the power supply.
3. Feed a square wave signal at the trigger input and sine wave at the control input.
4. Observe the input modulating signal, carrier pulse train and the PWM output signal on CRO. Vary the modulating signal amplitude to get the optimal output. Plot the waveforms.

WAVEFORMS:



(C) PPM

AIM: To set up pulse position (PPM) modulator and demodulator circuits and to observe and plot the waveforms.

COMPONENTS AND EQUIPMENTS REQUIRED:

Modulator

IC 555, Resistors, Capacitors, Diode 1N4001, CRO Signal Generator, Bread Board, Power Supply, Wires and connectors

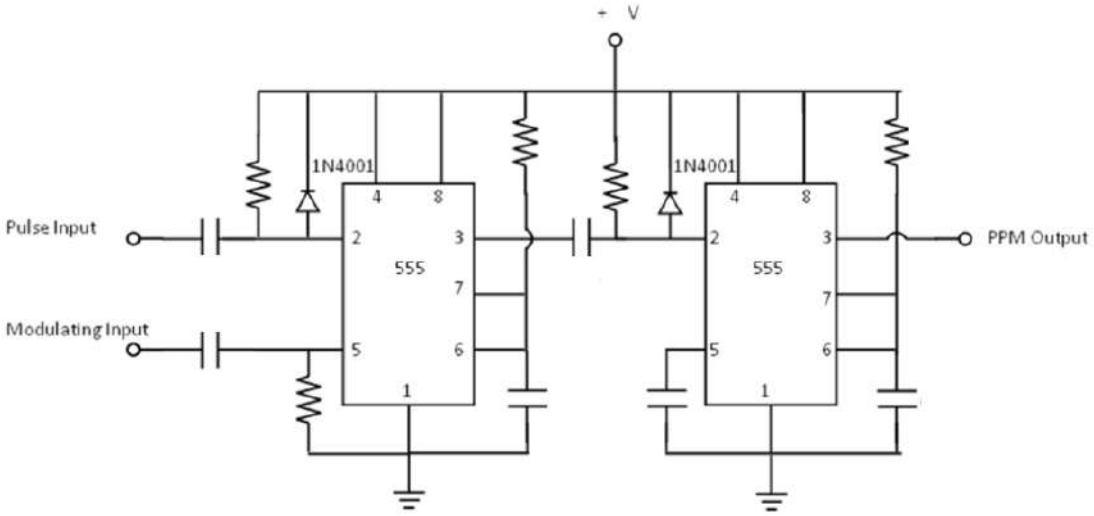
Demodulator

IC 741, IC LM324, Resistors, Capacitors, CRO, Bread Board, Power Supply, Wires and connectors

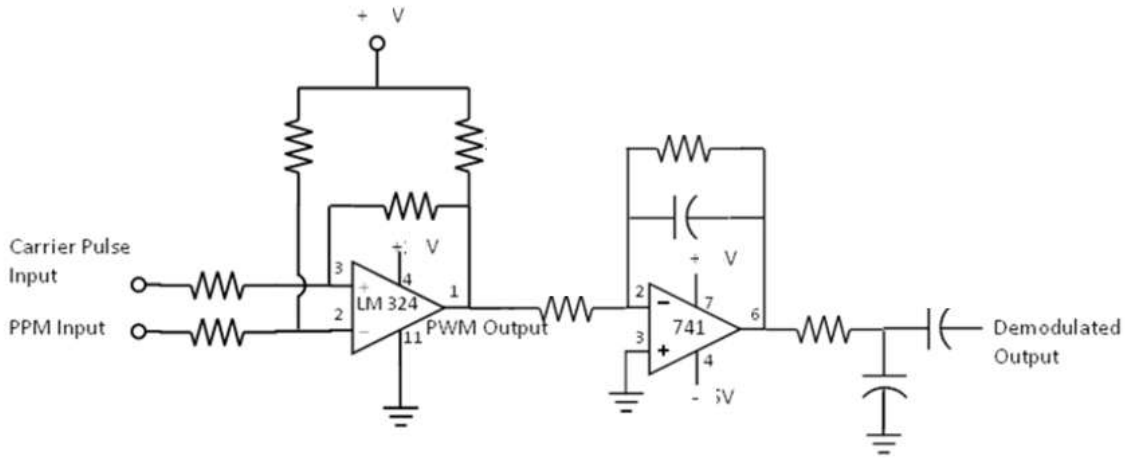
THEORY:

Pulse Position Modulation (PPM) is one of the pulse modulation schemes where the relative position of the pulses in a carrier pulse train is made proportional to the instantaneous value of the modulating signal. A pulse position modulator made up of IC 555 is shown in figure. Both the 555s are working in monostable mode. The first monostable generates a PWM signal and this PWM output is used as the trigger input of the second monostable. Since the monostable triggers at the trailing edge of the PWM signal, the position of the resulting pulses will have position shift compared to the input pulse train. The PPM demodulator is set up using an Op Amp SR flip flop, an integrator and a low pass filter. The flip flop is set by the carrier pulses and reset by the PPM pulses. The resulting output is a PWM signal. This PWM signal is then demodulated using the integrator-low pass filter combination.

CIRCUIT DIAGRAM:



Modulator



Demodulator

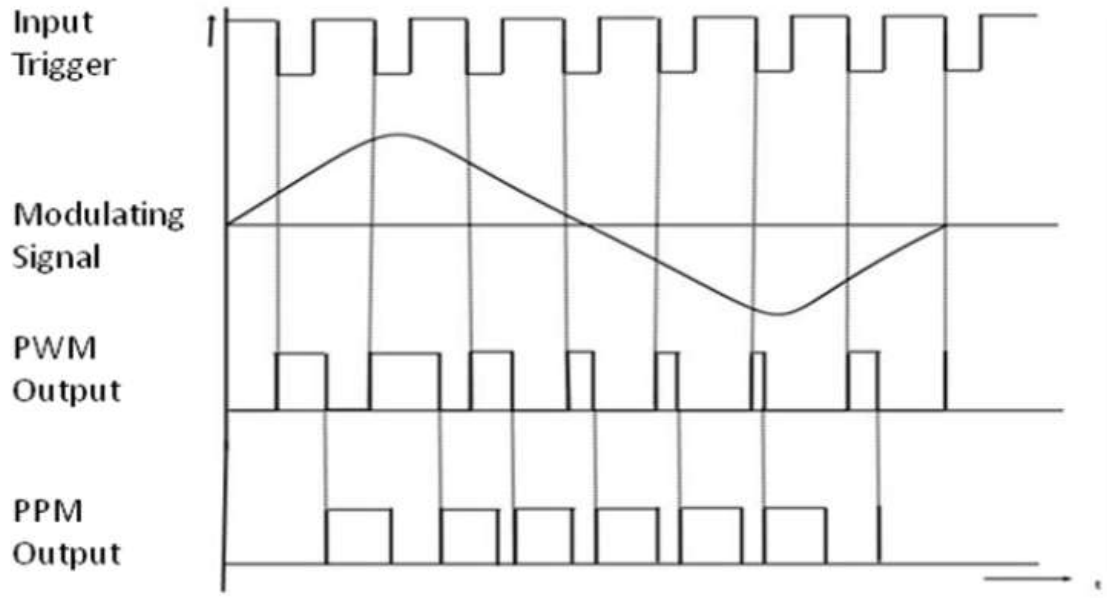
PROCEDURE:

1. Test all the components and probes.
2. Set up the circuit as shown in the figure on the bread board. Switch on the power supplies.
3. Feed a carrier pulse train and the modulating signal (Sine wave) at the trigger and control inputs of the first 555 respectively.
4. Make sure that the PWM signal is available at pin 3 of the first 555. Vary the amplitude of the modulating signal to get a proper PWM output if needed.
5. Observe the waveforms of the input pulse train, modulating input, PWM output and PPM output on the CRO.
6. Observe the following waveforms in pairs on both the channels of the CRO;
   a) Modulating input and PWM output b) PWM output and PPM output c) Modulating

input and PPM output

7. Plot the waveforms.
8. Set up the demodulator circuit as shown in figure. Switch on the power supply.
9. Feed the PPM signal input and the carrier pulse input as shown in figure. Observe the waveforms at various points on CRO and plot.

WAVEFORMS:



14. GENERATION AND DETECTION OF BPSK/DPSK

(A)BPSK

AIM: To design and setup a Binary Phase Shift Keying (BPSK) modulator

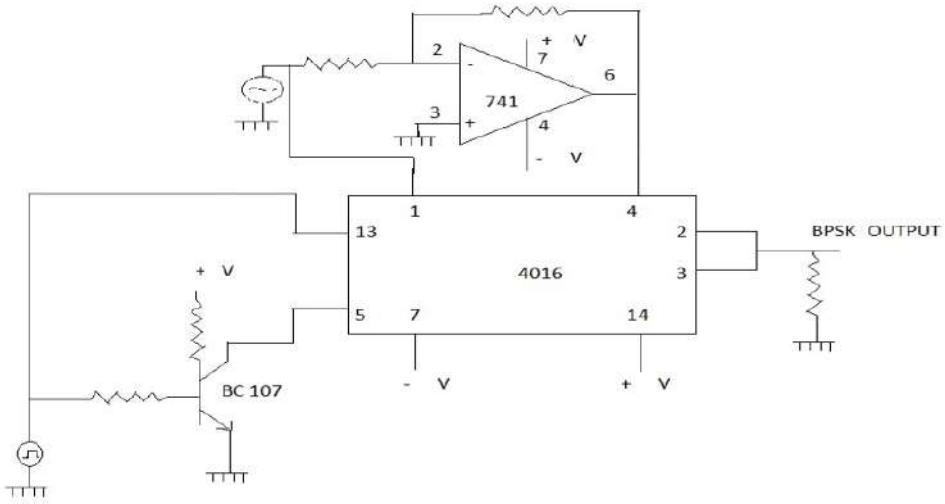
COMPONENTS AND EQUIPMENTS REQUIRED:

ICs 4016, 741, transistor, resistors, breadboard, function generator and CRO

THEORY:

In the BPSK system, out of phase signals are transmitted corresponding to the binary input. When the modulation input is at logic 1, a finite number of cycles of a sinusoidal signal are transmitted and when the input is at logic 0, phase of sinusoid is changed. Op-amp functioning as an inverting amplifier provides 180^o phase shift and unity gain. BPSK signal has constant amplitude as in the case of BFSK signal. Therefore the noise can be removed easily.

CIRCUIT DIAGRAM:



DESIGN:

Gain of inverting amplifier, A = - $\frac{RF}{Ri}$

Let the gain be -A so that the ratio $\frac{RF}{Ri}$ = A

Take appropriate values for $R_F = AR_i$

R_C and R_B are designed to bias the transistor as a switch. Select BC107 transistor. Take general assumptions of hfe and I_C

$R_C = \frac{VCC - VCE}{IC}$

Base current I_B should be greater than I_C/h_{fe} to function as a switch.

Take $I_B = 10 \times \frac{IC}{hfe}$

$R_B = \frac{5 - VBE}{IB}$

PROCEDURE:

1. Set up the circuit part by part and verify their function
2. Connect the parts together and observe output waveform on CRO screen

(B) DPSK

AIM: To study the various steps involved in the generation of Differential Phase Shift Keyed signal and also to recover the binary signal from the received DPSK signal.

COMPONENTS AND EQUIPMENTS REQUIRED:

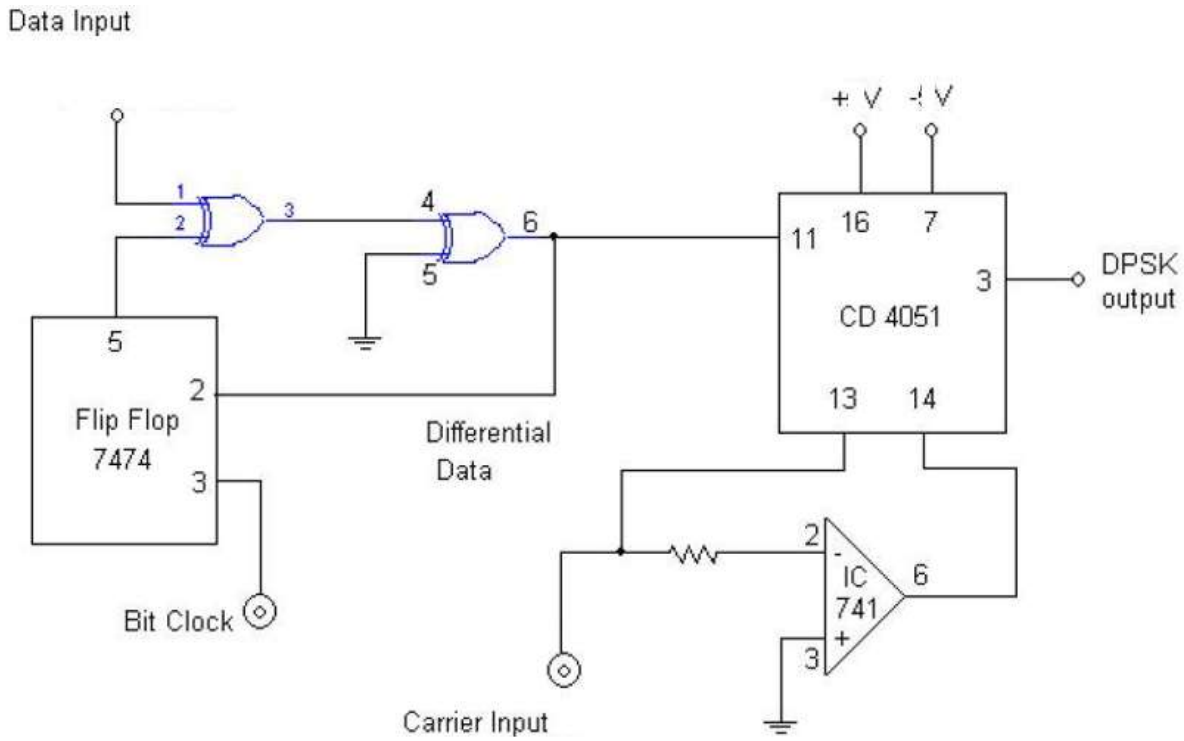
DPSK trainer board, CRO

THEORY:

The differentially coherent PSK signalling scheme makes use of a technique designed to get around the need for a coherent reference signal at the receiver. In the DPSK scheme, the phase reference for demodulation is derived from the phase of the carrier during the

preceding signalling interval, and the receiver decodes the digital information based on the differential phase.

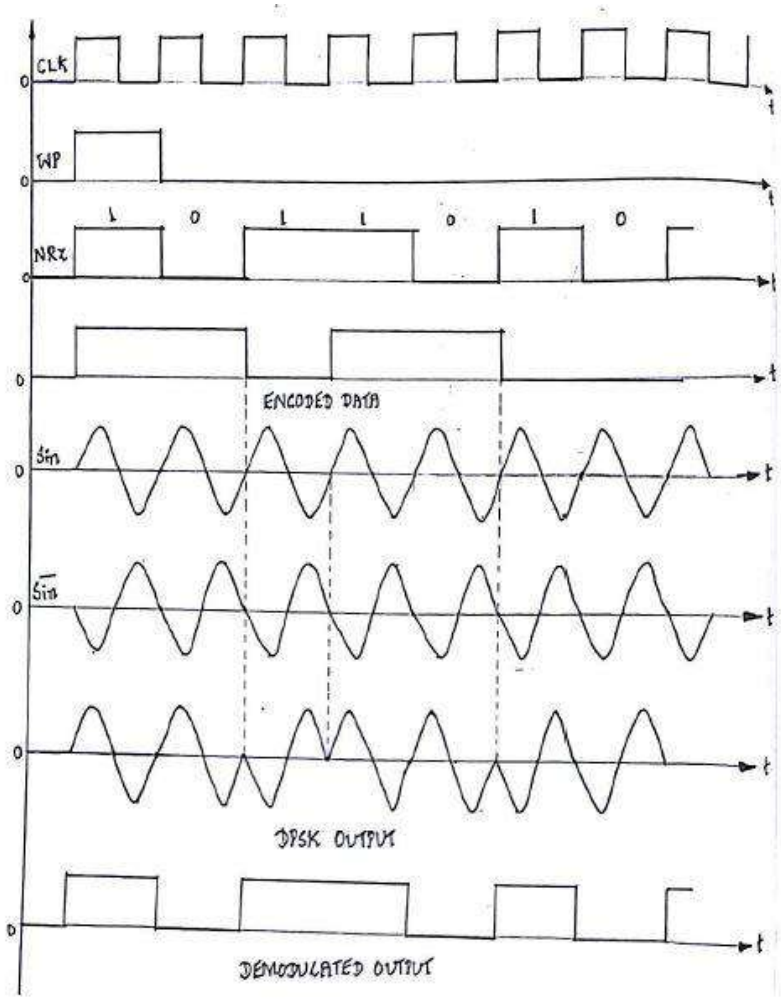
CIRCUIT DIAGRAM:



PROCEDURE:

1. Switch on the experimental board.
2. Check the carrier signal and the data generator signals initially.
3. Apply the carrier signal to the carrier input, the data input to the data input and bit clock to the DPSK modulator.
4. Observe the DPSK wave with respect to the input data generated signal of dual trace oscilloscope.
5. Give the output of the DPSK modulator signal to the input of demodulator, give the bit clock output to the bit clock input to the demodulator and also give the carrier output to the carrier input of demodulator.
6. Observe the demodulator output with respect to data generator signal.

MODEL WAVEFORMS:


CLK
WP
NRZ
1 0 1 1 0 1 0
ENCODED DATA
Sin
Sin
DPSK OUTPUT
DEMODULATED OUTPUT

15. GENERATION AND DETECTION OF PCM

AIM: To set up a PCM modulator and observe the waveforms.

COMPONENTS AND EQUIPMENT REQUIRED :

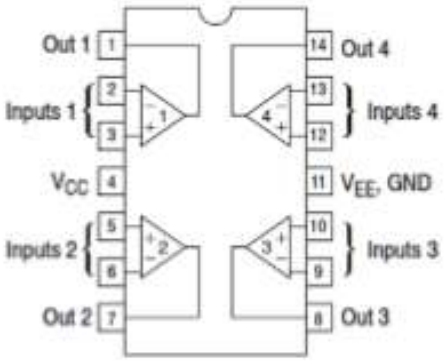
Op-amp, LM-324, analog switch, CD 4016, 4 bit counter, 74LS93, 7408, resistors, capacitors, dc source, signal generators, DSO.

THEORY:

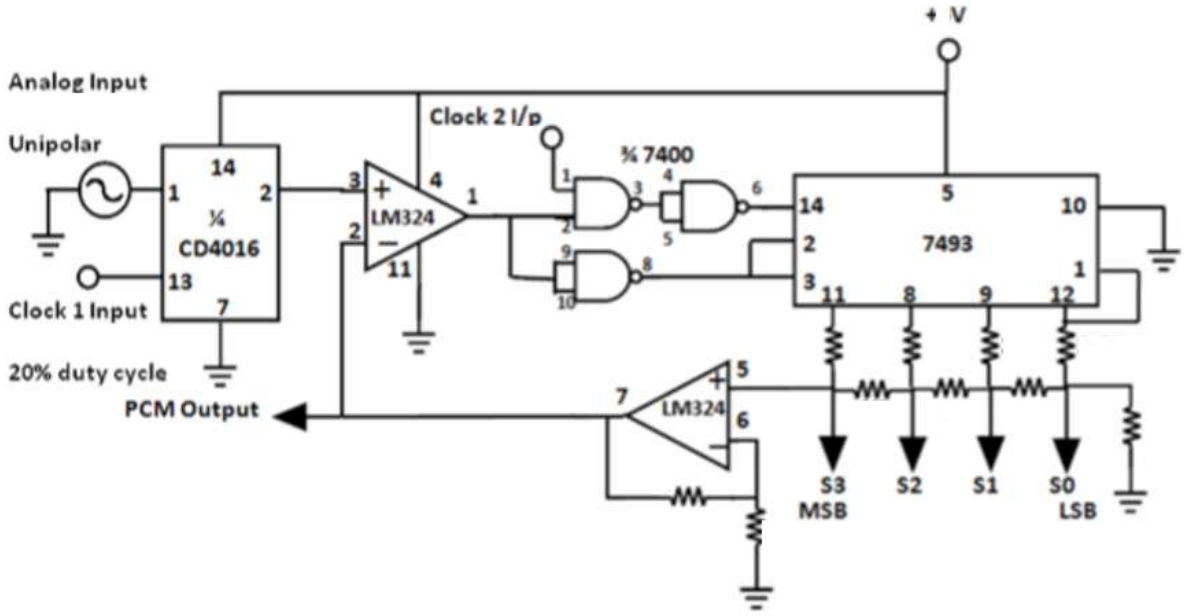
Pulse Code Modulation is a digital modulation technique by which an analog signal is converted to an equivalent sequence of binary codes. The analog signal is first sampled at regular intervals and these samples are then quantized to predefined levels. An analog to digital convertor converts these quantized symbols to their corresponding binary codes.

In the circuit an analog switch is used to sample the input signal. These samples are compared to the output of a DAC circuit which is initially zero. So the comparator output goes ‘high’ and strobes the clock input to the counter. This signal also disables the reset inputs of the counter. The counter starts to count up. An R-2R ladder DAC simultaneously converts the counter output to its equivalent analog value. When the DAC output goes above the input sample, the comparator output switches to ‘low’ and cuts off the clock input from the counter. The reset inputs are also enabled causing the counter output to reset. When the next sample reaches the comparator input the whole process starts over again.

CIRCUIT DIAGRAM:

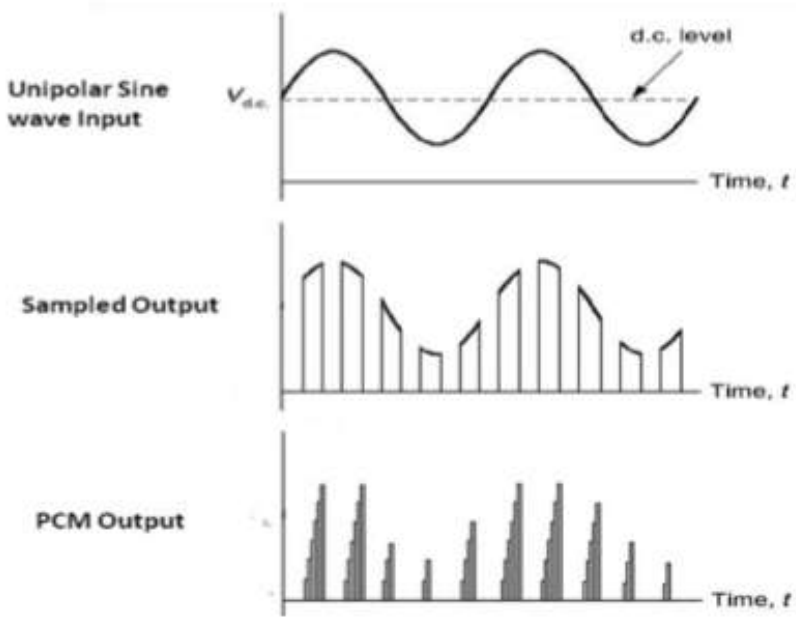


LM 324 Pin Connection



PCM Modulator

SAMPLE WAVEFORM:



PROCEDURE:

1. Test all the components and probes.
2. Set up the circuit as shown in figure on a bread board.
3. Feed unipolar sine wave as the analog input. Make sure that the input peak voltage never exceeds the peak DAC output.

4. Use the dc offset knob on the function generator to add dc offset to make unipolar sine wave.
5. Use a square wave with 20% duty cycle as sampling clock (clock 1) and another square wave as the clock input of the counter (clock 2).
6. Observe the input sine wave, sampled output and the PCM output (DAC output; staircase waveform) on CRO. Vary the analog input and clock 1 input amplitudes to obtain the optimum result, if needed.
7. Plot the waveforms.
8. The binary output can be checked by giving discrete dc input voltages (less than 5V).

16. QPSK MODULATION AND DEMODULATION

AIM: To study the generation and demodulation of a quadrature phase shift keyed (QPSK) signal.

COMPONENTS AND EQUIPMENT REQUIRED:

CRO, experimental kit, power supply, connecting leads

THEORY:

QPSK is a form of phase modulation technique, in which two information bits (combined as one symbol) are modulated at once, selecting one of the four possible carrier phase shift states. In binary PSK (BPSK), the change in logic level causes the BPSK signal's phase to change, it does so by 180^o.

A QPSK signal can be generated by independently modulating two carriers in quadrature as shown in the figure below:

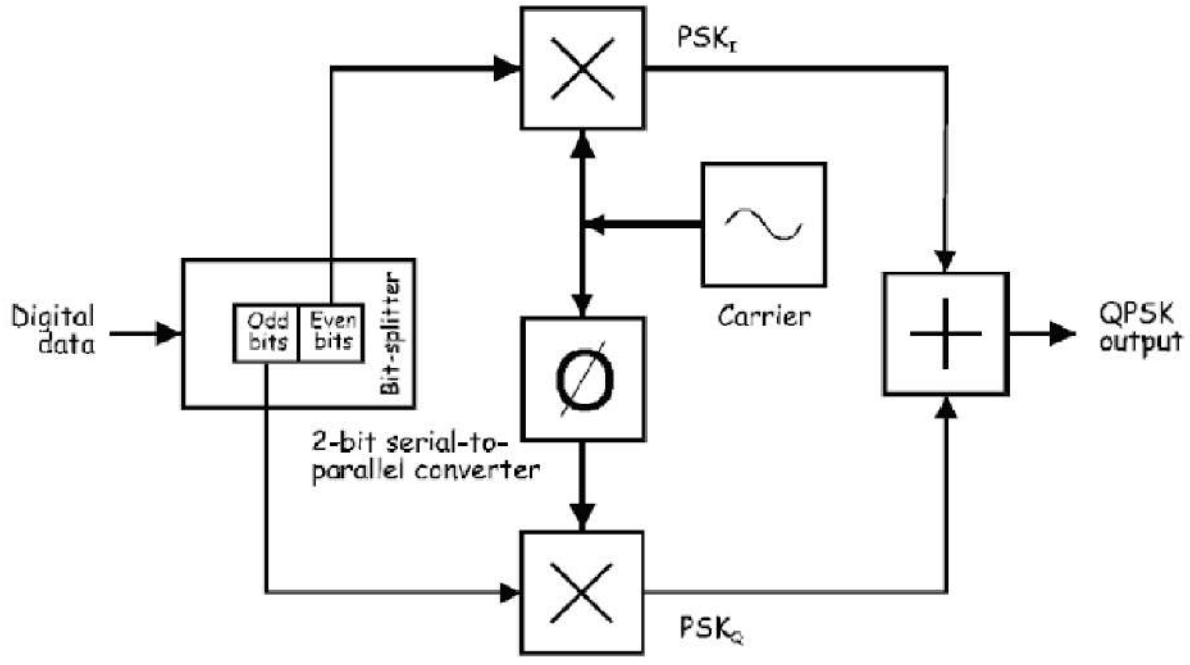


Figure: Block diagram of the mathematical implementation of QPSK

At the input to the modulator, the digital data's even bits (that is, bits 0, 2, 4 and so on) are stripped from the data stream by a "bit-splitter" and are multiplied with a carrier to generate a

BPSK signal (called PSK_I). At the same time, the data's odd bits (that is, bits 1, 3, 5 and so on) are stripped from the data stream and are multiplied with the 90° phase-shifted carrier to generate a second BPSK signal (called PSK_Q). The two BPSK signals are then simply added together for transmission.

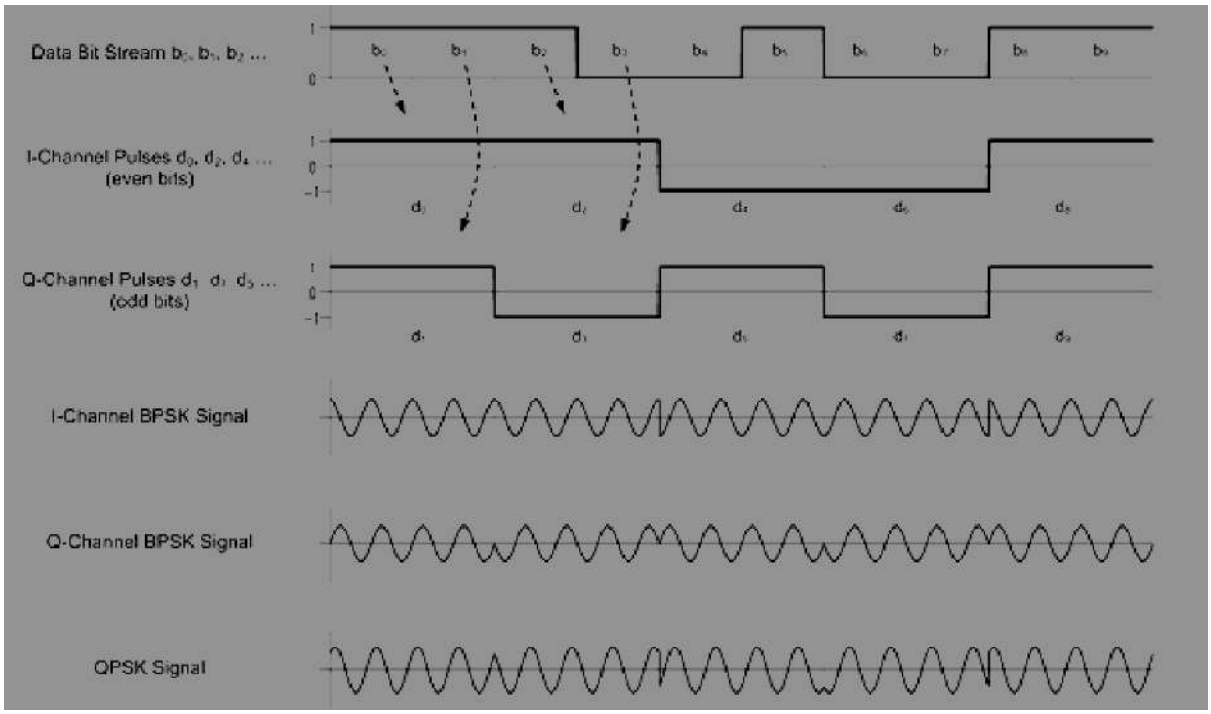


Figure: QPSK signal generation from two BPSK signals

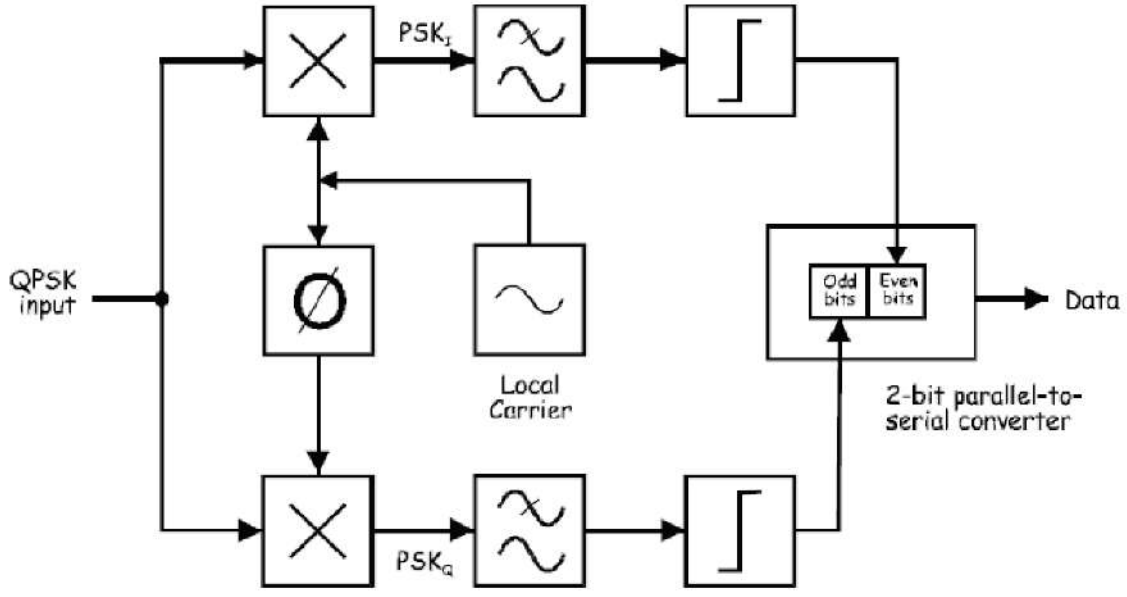


Figure: Block diagram of the mathematical implementation of QPSK demodulation

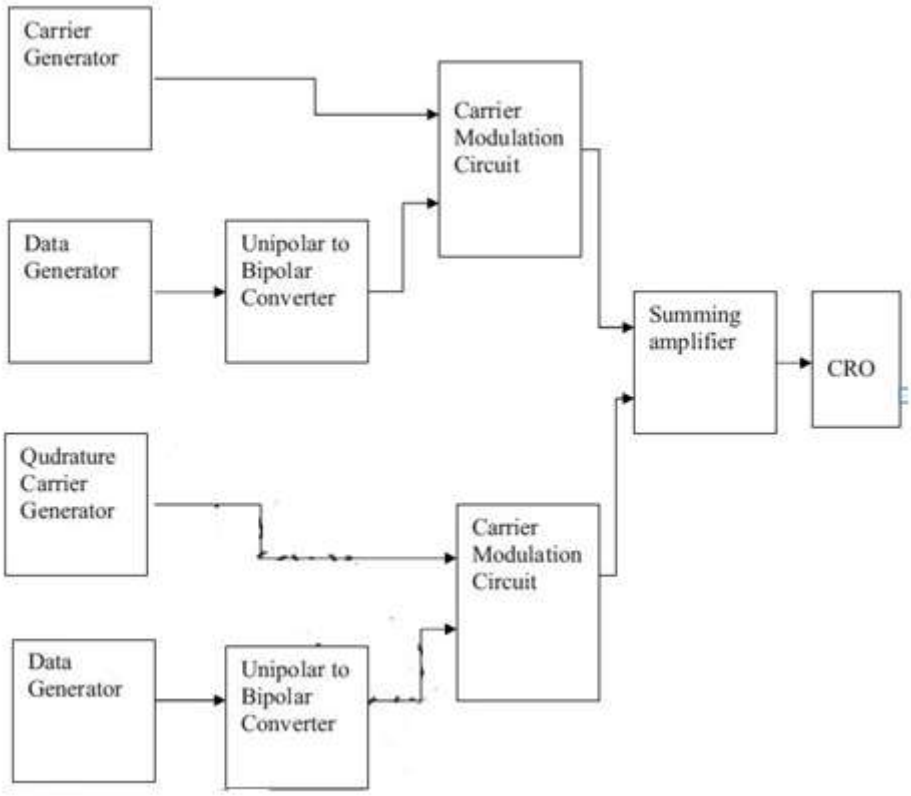
The arrangement uses two product detectors to simultaneously demodulate the two BPSK signals. This simultaneously recovers the pairs of bits in the original data. The two signals are cleaned-up using a comparator or some other signal conditioner then the bits are put back in order using a 2-bit parallel-to-serial converter.

An experimental kit, say, Emona Telecoms-Trainer 101 is used to generate a QPSK signal by implementing the mathematical model of QPSK. Once generated, the QPSK signal can be examined using the scope which clearly depicts how phase discrimination using a product detector can be used to pick-out the data on one BPSK signal or the other.

PROCEDURE:

1. Make the connection according to the block diagram.
2. Connect the modulator output to CRO.
3. Observe output on CRO

BLOCK DIAGRAM:



SAMPLE WAVEFORM: