DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COLLEGE OF ENGINEERING, THIRUVANANTHAPURAM

ECL 202: ANALOG CIRCUITS AND SIMULATION LAB

LAB MANUAL

PART A - EXPERIMENTS

Exp.No.1

RC INTEGRATOR AND DIFFERENTIATOR

AIM

1. To design and set up a RC integrator circuit, RC differentiator circuit and study the response to square wave.
2. To observe the response of the designed circuits for the given square waveform for RC<<T, RC=T, RC>>T.

COMPONENTS & EQUIPMENTS REQUIRED

Resistor
Capacitor
Function Generator
CRO
Bread board
Connecting Wires

THEORY

An RC integrator is constituted by a resistance in series and a capacitor parallel with the output. This circuit produces an output voltage that is proportional to the integral of the input. Here the time constant is very large in comparison with the time required for the input signal to change. Under this condition the voltage drop across C will be very small in comparison with the drop across R. The current is V_{in}/R since almost all current appears across R. Output voltage across C is

For RC>>τ, $V_C = V_0 = \frac{1}{RC}\int_0^{\tau} V_{in}dt$

Voltage drop across C increases as time increases. A square waveform has positive and negative excursions with respect to its reference zero. If the input is square wave, capacitor charges and discharges from negative voltage to the positive voltage and back.For the circuit to work as a good integrator $\theta=90^0$. As $\tan\theta=\omega RC$; tan90=infinity, which is practically impossible. Therefore a reasonable criterion for good integration is $\theta=89.4^0$ if $\theta=89.4^0$, $\omega RC=95.48^0$. So RC>16T will give the integrating practically.

An RC differentiator circuit is constituted with a capacitor connected in series and a resistor connected in parallel to the output. The time constant RC of the circuit is very small in comparison with the time period of the input signal. The voltage drop across R will be very small in comparison with the drop across C. The current through the capacitor is $C\frac{dVin}{dt}$.Hence the output is proportional to the derivative of the input. Output voltage across R is

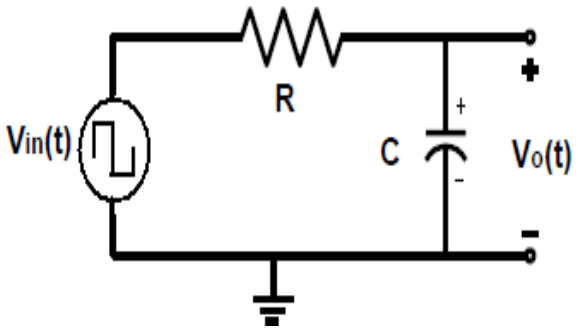
For RC<<τ, $V_0 = V_R = RC\ \frac{dV_{in}}{dt}$

Differentiated output is proportional to the rate of change of input. When the input rises to maximum value, differentiated output follows it because the sudden change of voltage is transferred to the output by the capacitor. Since the rate of change of voltage is positive, differentiated output is also positive. When input remains maximum for a period of time, the rate of change of voltage is zero. So, output falls to zero. During this time, input acts like a dc voltage and capacitor offers high impedance to it. So, the charges in capacitor drains to earth through the resistance. When input falls to zero, rate of change of input voltage is negative. Then the output also goes to negative.

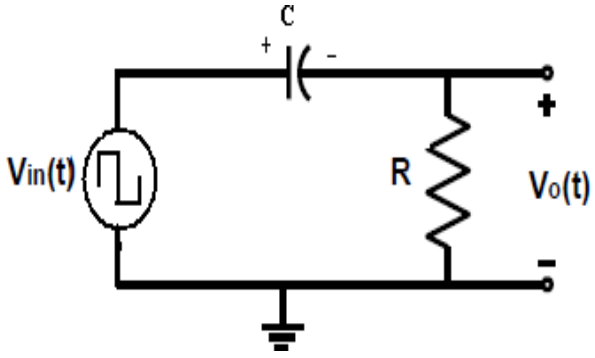
For the circuit to work as a good differentiator $\theta=90^0$. As $\tan\theta=1/\omega RC$; tan90=infinity. This result can be obtained only if R=0 or C=0, which is practically impossible. Therefore, a reasonable criterion for good differentiation is $\theta=89.4^0$ if $\frac{1}{\omega RC}=100$. So RC=0.0016T will give will give the differentiating practically. Assume RC=0.01T for getting good spike waveforms. The peak of the output of the differentiator gets doubled when the square wave is fed to the input.

CIRCUIT DIAGRAM

RC Integrator



RC Differentiator



DESIGN

RC Integrator

Case 1: RC>>T
To avoid loading, as a general assumption select R=10 times the output impedance of signal generation.

RC=10T

Case2: RC=T

Case3: RC<<T

RC=0.1T

Calculate capacitor value C as per given in the above three cases

RC Differentiator

Case 1: RC<<T
To avoid loading, select R=10 times the output impedance of signal generation.

RC=0.01T

Case2: RC=T

Case3:RC>>T

RC=5T

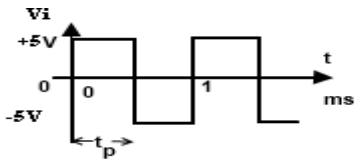
Calculate capacitor value C as per given in the above three cases

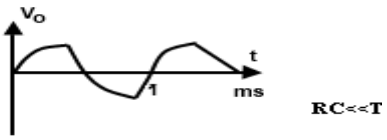
PROCEDURE

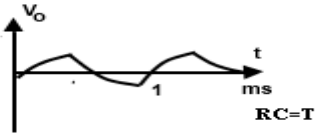
1. Set up the circuit as per the diagram of integrator.
2. Switch on the function generator and set a square wave output.
3. Observe the input and output on the X and Y channels of CRO respectively.
4. Note down the output waveforms for the following conditions:
    - RC<<T
    - RC=T
    - RC>>T (Integrator)
5. Repeat the same steps for differentiator.

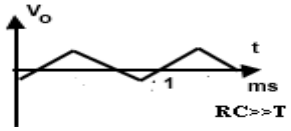
OUTPUT WAVEFORMS

Integrator

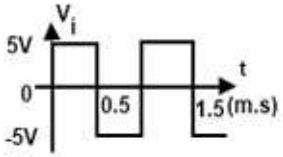


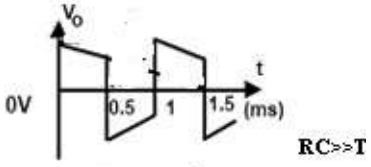


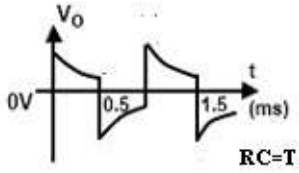


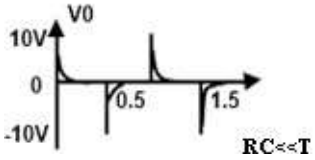


Differentiator









RESULT

RC Integrator and differentiator circuits are designed and observed the waveforms for different time constants.

Exp.No.2A

CLIPPING CIRCUITS

AIM

Design and setup various clipping circuits using diodes and plot the output waveform and transfer characteristics.

COMPONENTS & EQUIPMENTS REQUIRED

SL NO	COMPONENT
1	PN Diode
2	Zener diode
3	Resistors
4	CRO
5	DC source
6	Signal generator
7	Connecting wires
8	Bread board

THEORY

The property of a diode as a switching device is utilized in clipping circuits. Clipping circuits are linear wave shaping circuits. They are useful to clip off the positive or negative portions of an input waveform. It can also be used to slice off an input waveform between two voltage levels. Using a positive clipper, a moderate quality square waveform can be generated from a sine wave. The diode clippers can be classified as series and shunt clippers. If a diode is connected in series with input in a clipper, such a clipper is called a series clipper. If the diodes are connected in parallel with the input, thatclipper is called a shunt clipper. A resistance is used to limit the current through thediode. The value of the series resistance used in the clipping circuits is given by the expression :

$$R = \sqrt{R_f * R_r}$$

Where R_f= forward resistance of the diode and R_r = reverse resistance of the diode.

1. **Positive clipper with clipping level at 0.6V:**

   This circuit passes only negative going half cycles of the input to the output. The entire positive half cycle is bypassed through the diode since the diode gets forward biased when the input becomes positive. Due to the voltage drop across the diode the clipping occurs exactly at +0.6V.

2. **Negative clipper with clipping level at 0.6V:**

   This circuit passes only positive going half cycles of the input to the output. The entire negative half cycle is bypassed through the diode since the diode gets forward biased when the input becomes negative. Due to the voltage drop across the diode the clipping occurs exactly at -0.6V.

3. Positive clipper with clipping level at +2.6V :

For the diode to be forward biased anode voltage must be greater than cathode voltage. Till the input becomes greater than +2V, diode is reverse biased and the input will appear at the output. When the input exceeds +2V, diode becomes forward biased and the cell voltage appears at the output. Since the diode is in series with the cell, actual clipping level is +2.6V.

4. Negative clipper with clipping level at -2.6V :

Till the input becomes less than -2V, diode is reverse biased and the input will appear at the output. When the input is less than -2V, diode becomes forward biased and the cell voltage appears at the output. Since the diode is in series with the cell, actual clipping level is -2.6V.

5. Positive clipper with clipping level at -1.4V :

The diode is forward biased till the input becomes less than -1.4V .Here the cell voltage appears at the output. During the negative cycle when the input is less than -1.4V, diode is reverse biased and input appears at the output.

6. Negative clipper with clipping level at +1.4V :

During the positive cycle when the input is greater than +1.4V, diode is reverse biased and input appears at the output. Till the input becomes greater than +1.4V diode is forward biased and the cell voltage appears at the output.

7. Double clipper with clipping level at +3.6V & -2.6V :

This circuit is the merging positive and negative clippers. During the positive half cycle of the input, one branch will be effective and the other remains open and vice versa during negative half cycle. Actual clipping levels ate +3.6V and -2.6V.

8. Positive slicer with slicing level at +1.4V & +3.6V :

This circuit allows the signal to pass to the output only between +3V and +2V. During the negative half cycle of the input, diode D_1 conducts and diode D_2 gets reverse biased. Thus the output remains at +2V. During the positive half cycle of the input, when input exceeds +2V, D_1 is reverse biased and the input appears at the output. If the output exceeds +3V, diode D_2 conducts and the output remains at +3V. Actual clipping levels ate +1.4V and +3.6V.

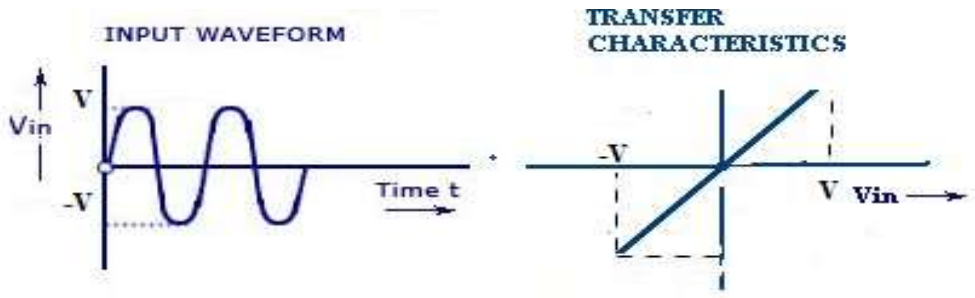
DESIGN

The series resistance used for current limiting

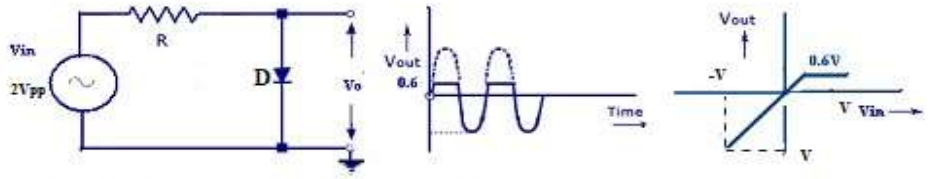
$$R = \sqrt{R_f * R_r}$$

Typical values of forward resistance R_f = 30 Ω and of R_r= 300 kΩ.$R = \sqrt{(30 \times 300k)}$ = 3k .Use 3.3 kΩ standard .

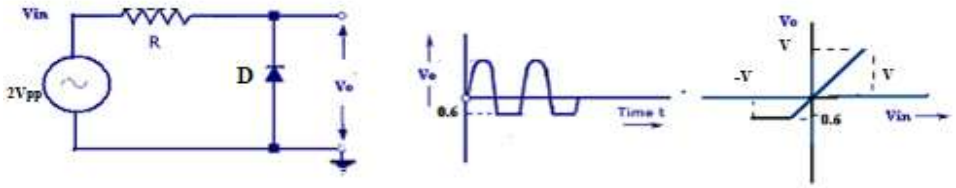
CIRCUIT DIAGRAM, WAVEFORMS & TRANSFER CHARACTERISTICS



1. Positive clipper with clipping level at 0.6V



2. Negative clipper with clipping level at 0.6V :



PROCEDURE

1. Set up the circuit as per the circuit diagram.
2. Apply 10Vpp,1 KHz input sine wave to the circuit from the signal generator.
3. Observe the output wave form on the CRO. Apply the input to X channel and output to channel Y and observe the waveforms simultaneously. Switch AC-DC coupling switch to DC mode.
4. To observe the transfer characteristics, keep the XY mode switch pressed and view the output.
5. Draw the output considering the diode drop.

RESULT

Various clipping circuits are studied and plotted the output waveforms and transfer characteristics

Exp.No.2B

CLAMPING CIRCUITS

AIM

Design and setup various clamping circuits using diodes and plot the output waveform and transfer characteristics.

COMPONENTS & EQUIPMENTS REQUIRED

SL NO	COMPONENT
1	PN Diode
2	Capacitor
4	CRO
5	DC source
6	Signal generator
7	Connecting wires
8	Bread board

THEORY

Clamping circuits are necessary to add or subtract a dc voltage to a given waveform without changing the shape of the waveform. A capacitor which is charged to a voltage and subsequently prevented from discharging can serve as a suitable replacement for a dc source. This principle is used in clamping circuits. The clamping level can be made at any voltage level by biasing the diode. Such a clamping circuit is called a biased clipper.

Suppose the input voltage is represented by the expression $V_m \sin\omega t$

1. **Positive clamper with clamping level at 0V :**

   During one negative half cycle of the input sine wave, the diode conducts and capacitor charges to V_m with positive polarity at right side of the capacitor. During positive half cycle of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor acts a dc source of V_m connected in series with the input signal source. The output voltage then can be expressed as $V_o = V_m + V_m \sin\omega t$ **.**

2. **Negative clamper with clamping level at 0V :**

   During one positive half cycle of the input sine wave, the diode conducts and capacitor charges to V_m with negative polarity at right side of the capacitor. During negative half cycle of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor acts a dc source of V_m connected in series with the input signal source. The output voltage then can be expressed as $V_o = -V_m + V_m \sin\omega t$.

3. **Positive clamper with clamping level at +3V :**

During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m+3) volts with positive polarity of the capacitor at the right side. The charging of the capacitor is limited to (V_m+3) volts due to the the presence of the dc source. The output is then V_o =(V_m+3)+$V_m$sinωt **.**

4. **Negative clamper with clamping level at -3V :**

During one positive half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m+3) volts with negative polarity of the capacitor at the right side. The charging of the capacitor is limited to (V_m+3) volts due to the the presence of the dc source. The output is then V_o =-(V_m+3) +$V_m$sinωt **.**

5. **Positive clamper with clampinglevel at -3V :**

During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m-3) volts with positive polarity of the capacitor at the right side. The charging of the capacitor is limited to (V_m-3) volts due to the the presence of the dc source. The output is then V_o =(V_m-3) +$V_m$sinωt **.**

6. **Negative clamper with clamping level at +3V :**

During one positive half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m-3) volts with negative polarity of the capacitor at the right side. The charging of the capacitor is limited to (V_m-3) volts due to the the presence of the dc source. The output is then V_o =-(V_m-3) +$V_m$sinωt **.**

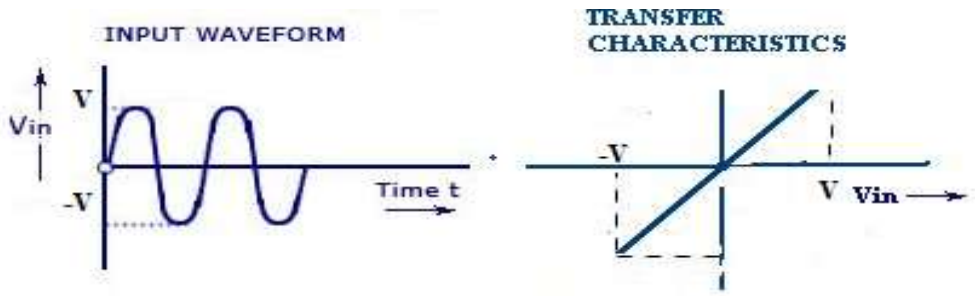
DESIGN

Use suitable value for capacitor C since it has to act like a voltage source.

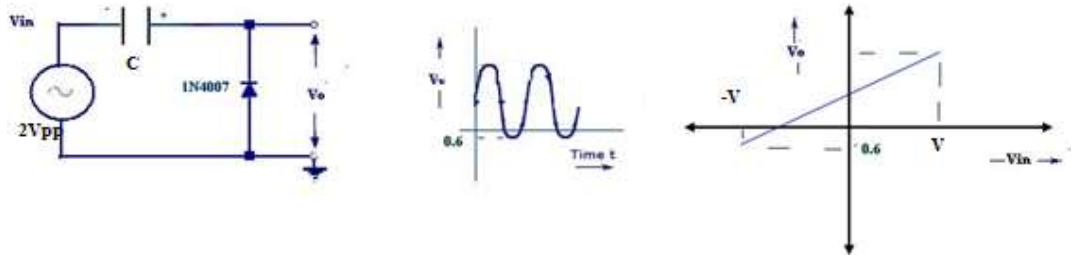
PROCEDURE

1. Set up the circuit as per the circuit diagram.
2. Apply 10Vpp, 1 KHz input sine wave to the circuit from the signal generator.
3. Observe the output wave form on the CRO. Apply the input to X channel and output to channel Y and observe the waveforms simultaneously. Switch AC-DC coupling switch to DC mode.
4. To observe the transfer characteristics, keep the XY mode switch pressed and view the output.
5. Draw the output considering the diode drop.

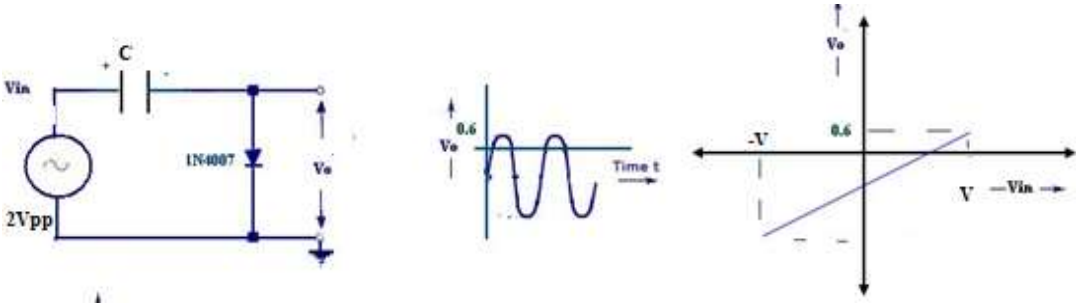
CIRCUIT DIAGRAM, WAVEFORMS & TRANSFER CHARACTERISTICS



1. **Positive clamper with clamping level at 0V**



2. **Negative clamper with clamping level at 0V**



RESULT

Various clamping circuits are studied and plotted the output waveforms and transfer characteristics

Exp.No.3

RC COUPLED AMPLIFIER

AIM

To design and set up an RC-coupled CE amplifier for a gain of A_V using bipolar junction transistorand to plot its frequency response.

COMPONENTS AND EQUIPMENTS REQUIRED

SL NO	COMPONENT
1	Resistor
2	Capacitor
3	Transistor
4	CRO
5	DC source
6	Signal generator
7	Connecting wires
8	Bread board

THEORY

RC-coupled CE amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter-base junction must be forward biased and the collector base junction must be reverse biased for the proper functioning of an amplifier. In the circuit diagram, an NPN transistor is connected as a common emitter ac amplifier. R_1 and R_2 are employed for the voltage divider bias of the transistor. Voltage divider bias provides good stabilisation independent of the variations of β. The input signal V_{in} is coupled through C_{C1} to the base and output voltage is coupled from collector through the capacitor C_{C2}. The input impedance of the amplifier isexpressed as $Zin = R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{FE}\, re))$ and output impedance as $Z_{out} = R_C \backslash\backslash R_L$ where $r_e$is the internal emitter resistance of the transistor given by the expression = 25 mV/I_E, where 25 mV is temperature equivalent voltage at room temperature.

Selection of transistor: Transistor is selected according to the frequency of operation, and power requirements. Low frequency gain of a BJT amplifier is given by the expression. Voltage gain $A_v = -h_{FE}RL/ Ri$. In the worst case with $R_L = R_i$; $A_V = -h_{F\,E}.h_{FE}$ of any transistor will vary in large ranges, for BC107 (an AF driver) varies from 100 to 500. Therefore a transistor must be selected such that its minimum guaranteed h_{FE} is greater than or equal to A_V required.

Selection of supply voltage: V_{CC} For a distortion less output from an audio amplifier, the operating point must be kept at the middle of the load line selecting V_{CEQ} = 50% V_{CC} (= 0:5V_{CC}). This means that the output voltage swing in either positive or negative direction is half of V_{CC} . However, V_{CC} is selected 20% more than the required voltage swing. For example, if the required output swing is 10 V, V_{CC} is selected 12 V.

Selection of collector current I_C: The nominal value of I_C can be selected from the data sheet. Usually it will be given corresponding to h_{FE} bias. It is the bias current at which h_{FE} is measured. For BC107 it is 2mA, for SL100 it is 150mA, and for power transistor 2N3055 it is 4 A.

Design of emitter resistor R_E: Current series feedback is used in this circuit using R_E. It stabilizes the operating point against temperature variation. Voltage across R_E must be as high as possible. But, higher drop across R_E will reduce the output voltage swing. So, as a rule of thumb, 10% of V_{CC} is fixed across R_E.

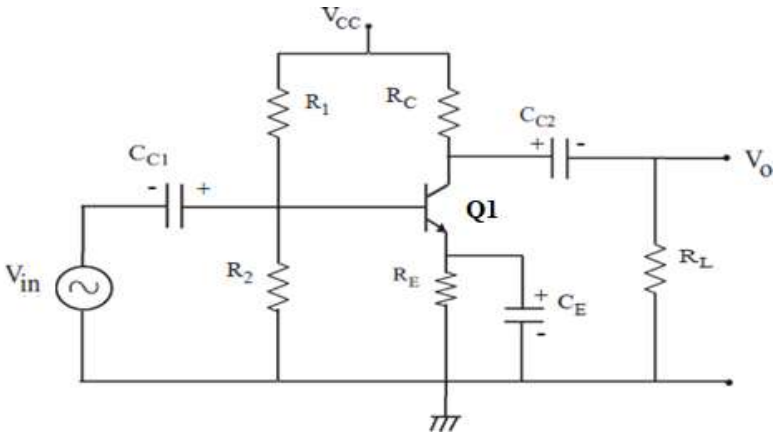
Design of R_C: Value of R_C can be obtained from the relation $R_C = 0.4V_{CC}/I_C$ since remaining 40% of V_{CC} is dropped across R_C.

Design of potential divider R_1 and R_2: Value of I_B is obtained by using the expression $I_B = I_C/h_{FEmin}$. At least $10I_B$ should be allowed to flow through R_1 and $9I_B$ through R_2 for the better stability of bias voltages. If the current through R_1 and R_2 is near to I_B, slight variation in I_B will a affect the voltage across R_1 and R_2. In other words, the base current will load the voltage divider. When I_B gets branched into the base oftransistor, $9I_B$ flows through R_2. Values of R_1 and R_2 can be calculated from the dc potentials created by the respective currents.

Design of bypass capacitor C_E: The purpose of the bypass capacitor is to bypass signal current to ground. To bypass the frequency of interest, reactance of the capacitor X_{CE} computed at that frequency should be much less than the emitter resistance. As a rule of thumb, it is taken $X_{CE} \leq R_E/10$.

Design of coupling capacitor C_C: The purpose of the coupling capacitor is to couple the ac signal to the input of the amplifier and block dc. It also determines the lowest frequency that to be amplified. Value of the coupling capacitor C_C is obtained such that its reactance X_C at the lowest frequency (say 100 Hz or so for an audio amplifier $\leq$ Rin/10. Here Rin = $R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}$ re) where re is the internal emitter resistance of the transistor given by the expression re= 25 mV/I_E at room temperature.

CIRCUIT DIAGRAM



DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = -h_{FE} R_L / Rin$ where $Rin = R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE} re)$

DC biasing conditions:

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,
V_{RC} = 40% of V_{CC}
V_{RE} = 10% of V_{CC}
V_{CE} = 50% of V_{CC}

Design of Rc:
$V_{RC} = I_C R_C$

Design of R_E:
$V_{RE} = I_E R_E$

Design of potential divider R_1 and R_2:

$I_B = I_C / h_{FE}$
With general assumptions take the current through R_1 as **10**I_B and that through R_2 as **9**I_B to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across $R_2 = V_{BE} + V_{RE} = 9 I_B R_2$

V_{R1}= Voltage across $R_1 = Vcc - V_{R2} = 10 I_B R_1$

Design for R_1 and R_2 from the above two equations

Design of R_L:

Gain of the common emitter amplifier is given by the expression $A_V = -(rc/re)$. Where rc $= R_C \backslash\backslash R_L$ and re = 25 mV/I_C.

From the above relations, we get $R_L = - A_V (R_C\, re)/ (R_C + re\, A_V)$

Design of coupling capacitor Cc_1 and Cc_2:

X_{C1} should be less than the input impedance of the transistor. Here, Rin is the input impedance.

With general assumption,
$X_{C1} \leq$ Rin /10.
where Rin = $R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}\, re)$
i.e. $Cc_1 \leq Rin/2\pi * f_L * 10$, where f_L is the lower cut-off frequency

Similarly, $X_{C2} \leq$Rout/10, where Rout = R_C
$Cc_2 \leq Rout/2\pi * f_L * 10$

Design of bypass capacitor C_E:

To bypass the lowest frequency, say f_{lo}, X_{CE} should be less than or equal to R_E
i.e., $X_{CE} \leq R_E/ 10$
$C_E \leq R_E/2\pi * f_{lo} * 10$

Circuit parameters	Design equations
R_1	$(Vcc- V_{BE} -V_{RE})\, h_{fe} / 10\, Ic$
R_2	$(V_{BE}+V_{RE})\, h_{fe} / 9\, Ic$
R_C	V_{RC} / I_C
R_E	V_{RE} / I_E
R_L	$- A_V (R_C\, re)/ (R_C + re\, A_V)$
C_{C1}	$\leq (R_1 \backslash\backslash\, R_2 \backslash\backslash (1+h_{fe}\, re))/2\pi * f_L * 10$
C_{C2}	$\leq R_C/2\pi * f_L * 10$
C_E	$\leq R_E/2\pi * f_{lo} * 10$

PROCEDURE

1. Test all the components using a multimeter. Set up the circuit and verify dc bias conditions. To check dc bias conditions, remove input signal and capacitors in the circuit.

2. Connect the capacitors in the circuit. Apply An input voltage (eg. 100 mV peak to peak sinusoidal signal) from the function generator to the circuit input. Observe the input and output waveforms on the CRO screen simultaneously.

3. Keep the input voltage constant and vary the frequency of the input signal from 0 to 1 MHz or highest frequency available in the generator. Measure the output amplitude corresponding to different frequencies and enter it in tabular column.

4. Plot the frequency response characteristics on a graph sheet with gain in dB on y-axis and logf on x-axis. Mark log f_L and log f_H corresponding to 3 dB points.

5. Calculate the bandwidth of the amplifier using the expression BW= f_H- f_L.

6. Remove the emitter bypass capacitor C_E from the circuit and repeat the steps 3 to 5 and observe that the bandwidth increases and gain decreases in the absence of C_E.

TABULAR COLUMN

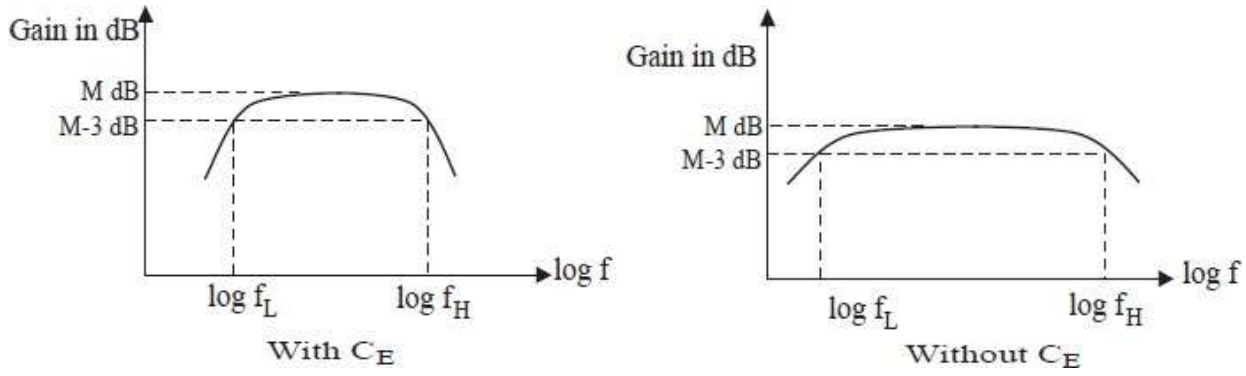
1) DC Conditions

DC CONDITIONS	V_{CC}	V_{R1}	V_{R2}	V_{RC}	V_{RE}	V_{CE}
Theoretical						
Practical						

2) Frequency Response

F (Hz)	V_o(v)	Log F	Gain(dB)=20log(V_o /V_{in})

EXPECTED GRAPH



RESULT

Designed and set up an RC coupled amplifier and studied its frequency response.

With C_E:

Mid-band gain of the amplifier = dB
Bandwidth of the amplifier = Hz

Without C_E:

Mid-band gain of the amplifier = dB
Bandwidth of the amplifier = Hz

Exp.No.4

RC PHASE SHIFT OSCILLATOR

AIM

To design and set up an RC phase shift oscillator using BJT for frequency f and observe the sinusoidal output waveform.

COMPONENTS AND EQUIPMENTS REQUIRED

SL NO	COMPONENT
1	Transistor
2	Capacitors
3	Resistors
4	Potentiometer
5	Breadboard
6	CRO
7	DC Source

THEORY

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is $A\beta = 1$ where A is the gain of the amplifier and β is the feedback factor. The unity gain means signal is in phase. (If the signal is 180 out of phase, gain will be 1.) If a common emitter amplifier is used, with a resistive collector load, there is a 180^0 phase shift between the voltages at the base and the collector. Feedback network between the collector and the base must introduce an additional 180^0 phase shift at a particular frequency.

In the figure shown, three sections of phase shift networks are used so that each section introduces approximately 60 phase shift at resonant frequency. By analysis, resonant frequency f can be expressed by the equation,

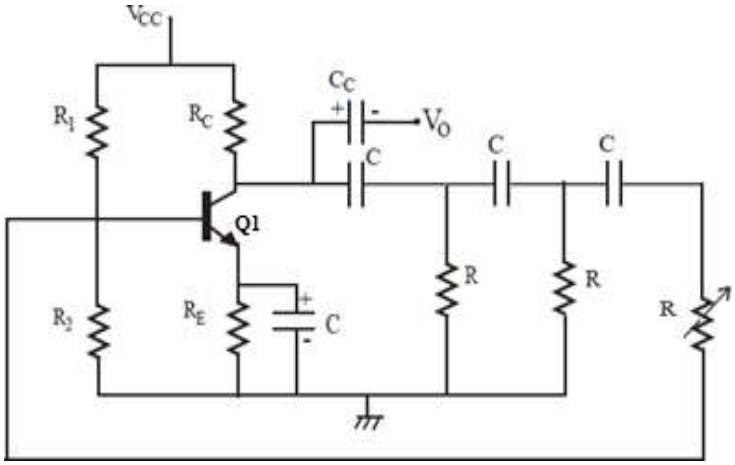
$$f = \frac{1}{2\pi RC\sqrt{(6 + 4(R_C/R))}}$$

The three section RC network offers a β of 1/29. Hence the gain of the amplifier should be 29. For this, the requirement on the h_{FE} of the transistor is found to be

$$h_{FE} \geq 23 + 29(R/R_C) + 4(R_C/R)$$

The phase shift oscillator is particularly useful in the audio frequency range.

CIRCUIT DIAGRAM



DESIGN

DC biasing conditions:

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,
V_{RC} = 40% of V_{CC}
V_{RE} = 10% of V_{CC}
V_{CE} = 50% of V_{CC}

Design of Rc:
V_{RC}= Ic Rc

Design of R_E:
V_{RE}= I_E R_E

Design of potential divider $R_1$and R_2:
I_B= I_C/ h_{FE}
With general assumptions take the current through R_1 as **10**I_B and that through R_2 as **9**I_B to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across R_2= V_{BE}+$V_{RE}$$V_{R2}$ = 9 I_B R_2

V_{R1}= Voltage across R_1= Vcc-V_{R2} =10 I_B R_1

Design for R_1 and R_2 from the above two equations

Design of bypass capacitor C_E:

To bypass the lowest frequency, say f_{lo}, X_{CE} should be less than or equal to R_E
i.e., $X_{CE} \leq R_E/ 10$
$C_E \leq R_E/2\pi * f_{lo}*10$

Design of frequency selective network:

$f = 1 / 2\pi RC \sqrt{(6 + 4 Rc/R)}$

The frequency determined by R and Rc must be selected in such a way to avoid loading of amplifier. So R is taken as 2Rc. From the value of R calculate C.

Circuit parameters	Design equations
R_1	$(Vcc- V_{BE} -V_{RE}) h_{fe} / 10 Ic$
R_2	$(V_{BE}+V_{RE}) h_{fe} / 9 Ic$
R_C	V_{RC} / I_C
R_E	V_{RE} / I_E
R_L	$- A_V (R_C re)/ (R_C + re A_V)$
C_E	$\leq R_E/2\pi * f_{lo}*10$
f	$1 / (2\pi RC \sqrt{(6 + 4 Rc/R)})$

TABULAR COLUMN

DC CONDITIONS

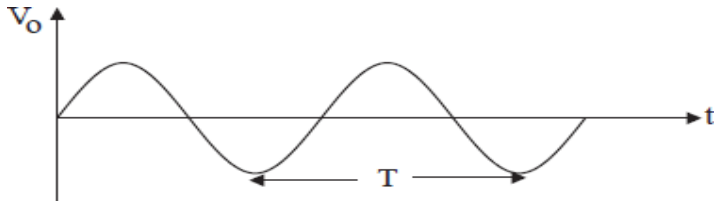
DC CONDITIONS	V_{CC}	V_{R1}	V_{R2}	V_{RC}	V_{RE}	V_{CE}
Theoretical						
Practical						

PROCEDURE

1. Set up the amplifier part of the oscillator and ensure that the transistor is operating as an amplifier.ie check the DC conditions.
2. Connect the feedback network and observe the sine wave on CRO and measure its amplitude and frequency.

MODEL GRAPH

OUTPUT WAVEFORM



RESULT

Designed and set up the RC phase shift oscillator and obtained the output waveforms.

Observed frequency =

PROGRAM No:5

COMMON SOURCE AMPILFIER

AIM: To verify the characteristics of common source amplifier for a voltage gain of A_V

COMPONENTS & EQUIPMENTS REQUIRED

Resistors, capacitors, transistor, power supply, function generator, connecting wires

THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P -N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate.

DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = gm(R_D \backslash\backslash R_L)$ where gm =transconductance

DC biasing conditions:

Voltage V_{GS} and current I_D are transistor dependent

With general assumptions,

$V_{RD} = V_{DS}$ =45% of V_{CC}

V_{RS}= 20% of V_{CC}

Design of R_D:

$V_{RD} = I_D R_D$

Design of R_S:

$V_{RS} = I_S R_S$, $I_S = I_D$ as current through gate is zero

Design of potential divider R_1 and R_2:

V_{R2}= Voltage across R_2= V_{GS}+V_{RS}= V_{DD}*(R_2/ R_1+ R_2)

Design R_2 from the above equation.

R_1 value should be large to ensure zero gate current.

Design of R_L:

Gain of the common source amplifier is given by the expression $A_V = gm(R_D \backslash\backslash R_L)$

i.e. $R_L = (gmR_D - A_V)/ R_D A_V$

Design of coupling capacitor Cc_1 and Cc_2:

X_{C1} should be less than the input impedance of the transistor. Here, gate impedance R_G is the input impedance.

With general assumption,
$X_{C1} \leq R_G /10$, R_G is in M Ω range
i.e., $Cc_1 \leq R_G / 2\pi * f_L * 10$, where f_L is the lower cut-off frequency

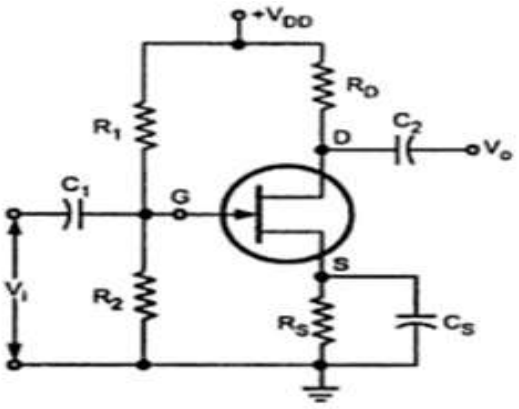
Similarly, $X_{C2} \leq R_D /10$, where
$Cc_2 \leq R_D /2\pi * f_L * 10$

Design of bypass capacitor C_S:

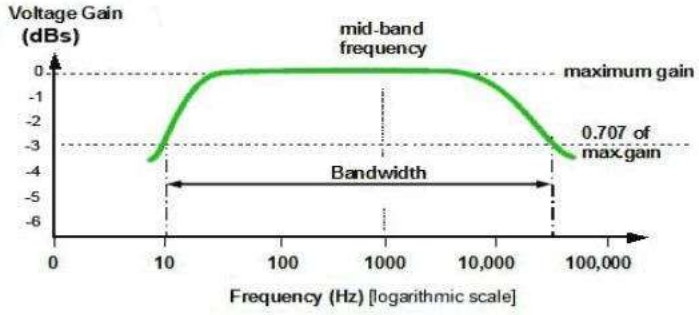
To bypass the lowest frequency, say f_{lo}, X_{CS} should be less than or equal to R_E
i.e., $X_{CS} \leq R_S/ 10$
$C_S \leq R_S/2\pi * f_{lo} * 10$

Circuit parameters	Design equations
R_1	M Ω range
R_2	$R_1/((V_{DD}/(V_{GS}+V_{RS}))-1)$
R_D	V_{RD} / I_D
R_S	V_{RS} / I_D
R_L	$(gmR_D - A_V)/ R_D A_V$
C_{C1}	$\leq R_G /(2\pi * f_L * 10)$
C_{C2}	$\leq R_C/(2\pi * f_L * 10)$
C_E	$\leq R_E/(2\pi * f_{lo} * 10)$

CIRCUIT DIAGRAM



MODEL GRAPH



RESULT

Designed and set up a common source amplifier and studied its frequency response.

Mid-band gain of the amplifier = dB
Bandwidth of the amplifier = Hz

PROGRAM No:6

CASCADE AMPLIFIER

AIM: To design a cascade amplifier for a gain of A_V and obtain the transient response and frequency response.

COMPONENTS REQUIRED

Transistors, Resistors, Capacitors, Voltage source, connecting wires

THEORY

A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times, the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker.

DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = A_{V1} * A_{V2}$ where A_{V1} and A_{V2} are voltage gain of first stage and second stage respectively.
A_{V1} should be larger than A_{V1} to avoid high input voltage to second stage.

$A_{V1} = (R_C \backslash\backslash R_{in2})/(re+R_{e1})$ where $re = 25\ mV/I_C$ and $R_{e1} = R_E - R_e$[1]
and $R_{in2} = R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{fe}\, re)$
and $A_{V2} = (Rc \backslash\backslash R_L)/re$

DC biasing conditions:

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,
V_{RC} = 40% of V_{CC}
V_{RE} = 10% of V_{CC}
V_{CE} = 50% of V_{CC}

Design of R_{C1} and R_{C2}:

$V_{RC} = Ic\ Rc$
Choose Rc1= Rc2

Design of potential divider R_1 and R_2:

$I_B = I_C / h_{FE}$
With general assumptions take the current through R_1 as **10**I_B and that through R_2 as **9**I_B to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across $R_2 = V_{BE} + V_{RE} = 9\ I_B\ R_2$

V_{R1}= Voltage across $R_1 = Vcc - V_{R2} = 10\ I_B\ R_1$

Design for R_1 and R_2 from the above two equations
Choose $R_{11} = R_{21}$ and $R_{12} = R_{22}$

Design of R_{E1} and R_{E2}

R_{E1} of first stage is split into R_e and R_e^1
$V_{RE1} = I_E\ R_{E1} = I_C\ R_{E1}$
Find R_{E1} from above relation. Choose $R_{E1} = R_{E2}$
$A_{V1} = (R_C \backslash\backslash R_{in2})/(re + R_{e1})$
Substituting for A_{V1}, R_C, R_{in2}, re the value for R_{e1} can be calculated.
Then from equation $R_{e1} = R_E - R_e^1$, value for R_e^1 can be calculated.

Design of R_L:

Gain of second stage $A_{V2} = (Rc \backslash\backslash R_L)/re$

From the above relations, we get $R_L = (R_C - A_{V2}\ re)/ (R_C\ re\ A_{V2})$

Design of coupling capacitor Cc_1, Cc_2 and Cc_3:

X_{C1} should be less than the input impedance of the transistor. Here, Rin is the input impedance.

With general assumption,
$X_{C1} \leq Rin/10$.
where $Rin = R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}\ re)$
i.e., $Cc_1 \leq Rin/2\pi * f_L * 10$, where f_L is the lower cut-off frequency

Choose $Cc_1 = Cc_2$

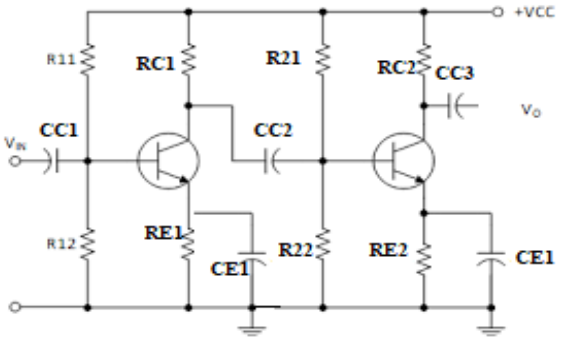
Similarly, $X_{C3} \leq Rout/10$, where $Rout = R_C$
$C_{C3} \leq Rout/2\pi * f_L * 10$

Design of bypass capacitor C_{E1} and C_{E2}:

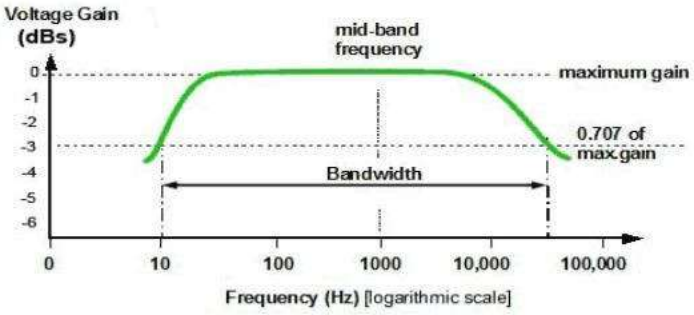
To bypass the lowest frequency, say f_{lo}, X_{CE} should be less than or equal to R_E
i.e., $X_{CE} \leq R_E/10$
$C_E \leq R_E/2\pi * f_{lo} * 10$
Choose $C_{E1} = C_{E2}$

Circuit parameters	Design equations
$R_{11} = R_{21}$	$(Vcc- V_{BE} -V_{RE}) h_{fe} / 10 Ic$
$R_{12} = R_{22}$	$(V_{BE}+V_{RE}) h_{fe} / 9 Ic$
$R_{C1}= R_{C2}$	V_{RC} / I_C
$R_{E1} = R_{E2}$	V_{RE} / I_E
R_L	$(R_C -A_{V2} re)/ (R_C re A_{V2})$
$C_{C1} = C_{C2}$	$\leq (R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{fe} re))/2\pi * f_L*10$
C_{C3}	$\leq R_C/2\pi * f_L*10$
$C_{E1} = C_{E2}$	$\leq R_E/2\pi * f_{lo}*10$

CIRCUIT DIAGRAM



MODEL GRAPH



Result

Designed and set up a cascade amplifier and studied its frequency response.

Mid-band gain of the amplifier = dB
Bandwidth of the amplifier = Hz

Exp.No.7

SERIES VOLTAGE REGULATOR

AIM

To design a series voltage regulator to obtain an output DC voltage of V from 8-12V DC input. The maximum load current is 50mA. Obtain line and load regulation graphs.

COMPONENTS REQUIRED

Transistor
Zener diode
Rheostats
Resistor
Voltmeters 0-10V
Ammeters 0-200mA
Regulated Power Supply
Bread board
Connecting Wires

THEORY

Voltage regulator is a device designed to maintain the output voltage as nearly constant as possible. It monitors the output voltage and generates feed back that automatically increases are decreases the supply voltage to compensate for any changes in output voltage that might occur because of change in load are changes in load voltages.

In transistorized series voltage regulator the control element is a transistor which is in series with load. It is a circuit that combines a zener regulator and an emitter follower. The zener diode must be operated in reverse break down region, where it provides constant voltage irrespective of changes in applied voltages. The output voltage of the series voltage regulator is $Vo = Vz - V_{BE}$. Since, Vz is constant; any change in Vo must cause a change in V_{BE} in order to maintain the above equation. So, when Vo decreases V_{BE} increases, which causes the transistor to conduct more and to produce more load current, this increase in load causes an increase in Vo and makes Vo as constant. Similarly, the regulation action happens when Vo increases.

The series resistance should be selected between Rs_{min} and Rs_{max} given by the expression.

$$Rs_{min}=(Vi_{(min)} - Vz)/I_s$$
$$Rs_{max}=(Vi_{(max)} - Vz)/I_s$$

DESIGN

Requirements: V_{out}=V, load current I_L

Selection of R_L:

R_L=Vout/Iz= V/ I_L

Power rating of $R_L = I_L^2 R_L$

Selection of R_B:

$R_{Bmax}=V_{inmax}-V_z/(I_{z(min)}+I_B)$

$R_{Bmin}=V_{inmin}-V_z/(I_{z(max)}+I_B)$

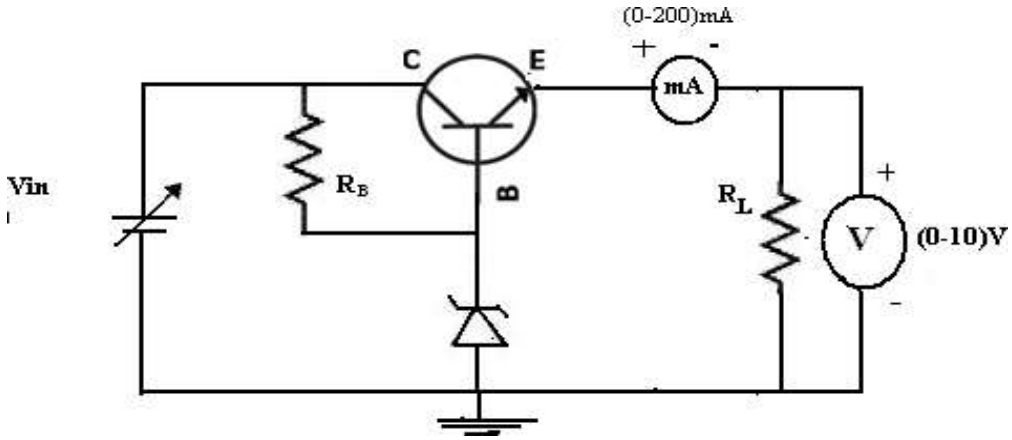
$R_B=(R_{Bmax}+R_{Bmax})/2$

Selection of R_L (Load regulation):

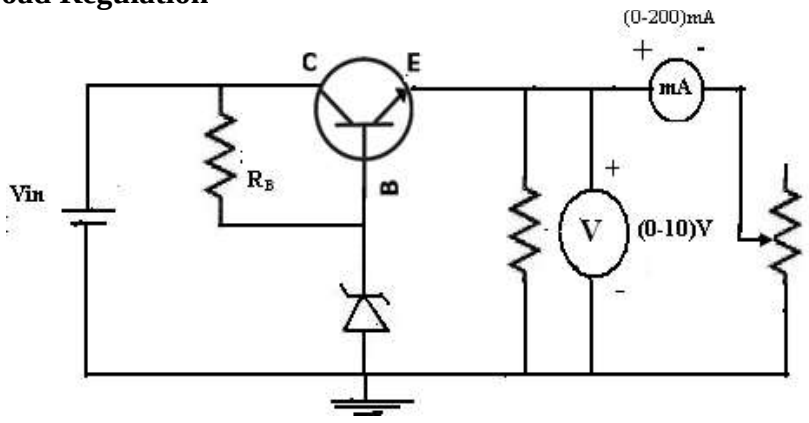
$R_L=V/I_L$

CIRCUIT DIAGRAM

i) Line Regulation



ii) Load Regulation



PROCEDURE

i). Line Regulation

1. Connect the circuit as shown in the circuit diagram.
2. Note down the output voltage when the input voltage varies from 8 to 12 V in steps of 1V.
1. Plot the line regulation graph V_{in} along x-axis and V_{out} along y-axis.
2. Calculate the percentage line regulation using expression $\Delta V_{out}/ \Delta V_{in}$.

ii). Load Regulation

1. Connect the circuit as shown in the circuit diagram.
2. Keep the input voltage as constant ie 10V.
3. Note down the output voltage when the load current varies from 0mA(NL) to 100mA(FL) by varying rheostat.
3. Plot the load regulation graph I_L along x-axis and Vout along y-axis.
4. Calculate the percentage load regulation using expression

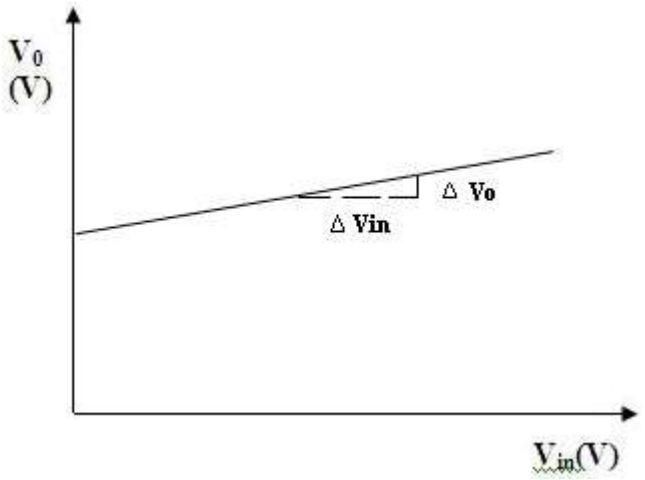
$$\text{Percentage load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} x100$$

OBSERVATION COLOUMN & CALCULATIONS

i) Line Regulation

I_L=…..mA

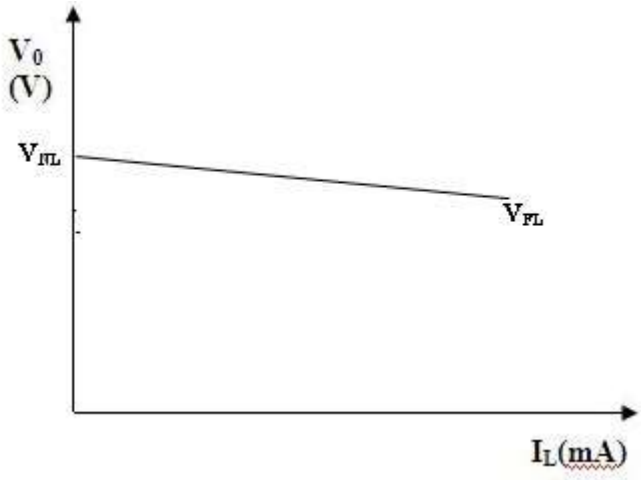
Vin(V)	**Vo(V)**



ii) Load Regulation

Vin=…..V

IL(mA)	**Vo(V)**



CALCULATIONS

$$\text{Percentage load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} x100 =$$

Percentage Line Regulation = (change in output) / (change in input) X 100

RESULT

Series voltage regulator circuit is set up and studied. Plotted load and line regulation characteristics.

% Line Regulation =…..
% Load Regulation =……

Exp.No.8

FEEDBACK AMPLIFIERS

AIM

To design and set up voltage series and current series feedback amplifiers and to plot its frequency response.

COMPONENTS REQUIRED

Sl.No.	Name
1.	Transistor
2.	Resistor
3.	Capacitor
4.	Function generator
6.	Regulated power supply
7.	Bread Board

THEORY

The phenomenon of feeding a portion of the output signal back to the input circuit is known as feedback. The effect results in a dependence between the output and the input and an effective control can be obtained in the working of the circuit. Feedback is of two types. Positive Feedback and Negative Feedback. In positive feedback, the feedback energy (voltage or currents), is in phase with the input signal and thus aids it. Positive feedback increases gain of the amplifier also increases distortion, noise and instability. Because of these disadvantages, positive feedback is seldom employed in amplifiers. In negative feedback, the feedback energy (voltage or current), is out of phase with the input signal and thus opposes it. Negative feedback reduces gain of the amplifier. It also reduces distortion, noise and instability. This feedback increases bandwidth and improves input and output impedances. Due to these advantages, the negative feedback is frequently used in amplifiers. The effect of negative feedback on an amplifier is considered in relation to gain, gain stability, distortion, noise, input/output impedance and bandwidth and gain-bandwidth product.

DESIGN

DC biasing conditions

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,

V_{RC} = 40% of V_{CC}

V_{RE} = 10% of V_{CC}

V_{CE} = 50% of V_{CC}

Design of Rc:

V_{RC}= Ic Rc

Design of R_E:

V_{RE}= I_E R_E

Design of potential divider $R_1$and R_2:

I_B= I_C/ h_{FE}

With general assumptions take the current through R_1 as **10**I_B and that through R_2 as **9**I_B to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across R_2= V_{BE}+$V_{RE}$$V_{R2}$ = 9 I_B R_2

V_{R1}= Voltage across R_1= Vcc-V_{R2} =10 I_B R_1

Design for R_1 and R_2 from the above two equations

Minimum operating frequency, f = 50 Hz

Xcc=10% Rc = 1/(2pi*f*Cc). Find value of Cc.

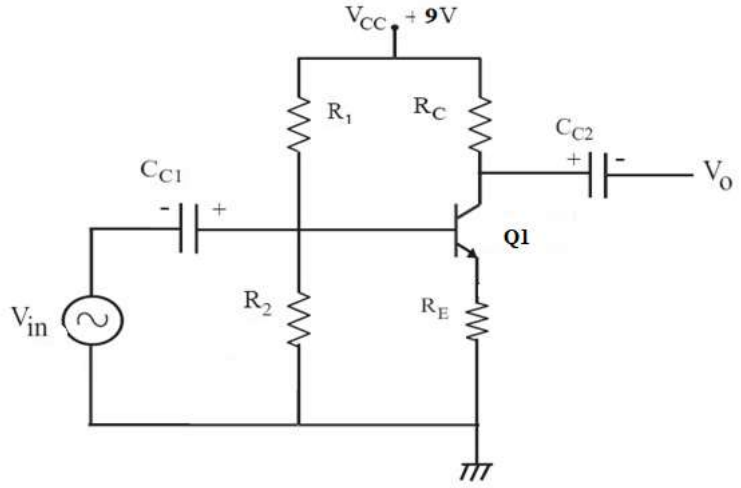
Circuit parameters	Design equations
R_1	(Vcc- V_{BE} -V_{RE}) h_{fe} / 10 Ic
R_2	R_1/((V_{DD}/(V_{GS}+V_{RS}))-1)
R_C	V_{RC} / I_C
R_E	V_{RE} / I_E
R_L	- A_V (R_C re)/ (R_C + re A_V)
C_{C1}	≤ (R_1\\ R_2\\(1+h_{fe} re))/2π * f_L*10
C_{C2}	≤ R_C/2π * f_L*10

PROCEDURE

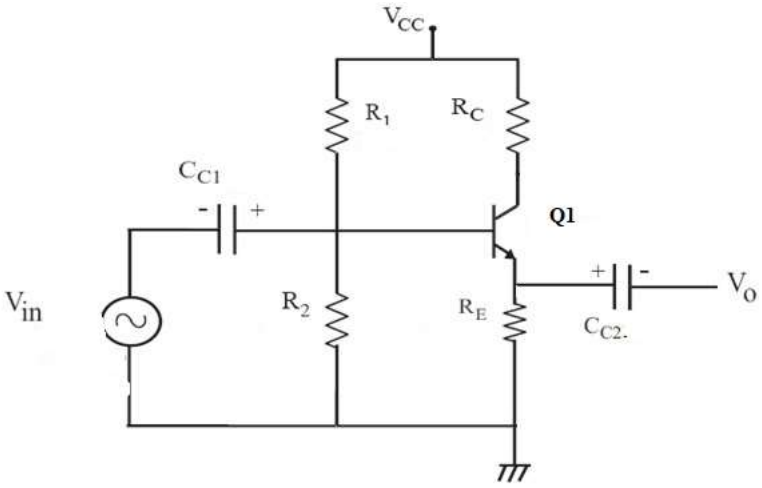
1. Set up the current series feedback amplifier as per circuit diagram, and give dc and ac signal.
2. Check dc conditions to ensure transistor is properly biased.
3. Note down the output amplitude for 20 mV_{p-p} signal for various frequencies and calculate gain for each reading.
4. Plot the frequency response characteristics on a graph sheet with gain in dB on yaxis and log f on x-axis. Mark log f_L and log f_H corresponding to 3 dB points.
5. Calculate the bandwidth of the amplifier.
6. Repeat the above steps for voltage series feedback amplifier.

CIRCUIT DIAGRAM

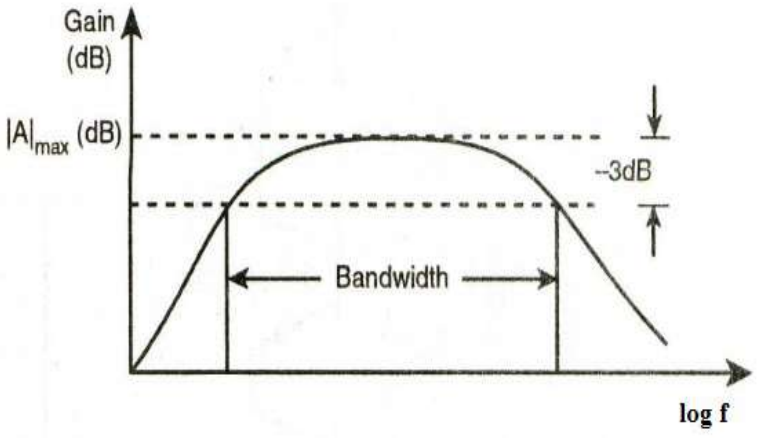
Current Series feedback amplifier



Voltage series feedback amplifier



FREQUENCY RESPONSE



CALCULATIONS

Current series feedback amplifier

Lower cut-off frequency, f_1 =
Upper cut-off frequency f_2 =
Bandwidth, B = $f_2 - f_1$

RESULT

Voltage series and current series feedback amplifiers are designed and set up. Frequency response is plotted and bandwidth is calculated as

Bandwidth =

Mid-band gain =

PART B - SIMULATIONS

PROGRAM: 1A

CLIPPING CIRCUITS

AIM: Design and setup various clipping circuits using diodes and plot the output waveform and transfer characteristics.

COMPONENTS REQUIRED

Diodes, Resistors, Voltage source, connecting wires

THEORY

The Diode Clipper, also known as a Diode Limiter, is a wave shaping circuit that takes an input waveform and clips or cuts off its top half, bottom half or both halves together. This clipping of the input signal produces an output waveform that resembles a flattened version of the input. For example, the half-wave rectifier is a clipper circuit, since all voltages below zero are eliminated.

There are two types of clippers namely series and parallel. In series clipper, diode is connected in series with the load. In parallel clipper, diode is in parallel to the load. Sometimes it is desired to remove a small portion of both positive and negative half cycles. In such cases, the dual clippers are used. The double clippers are made by combining the biased parallel positive clipper and biased parallel negative clipper. The resistor is mainly used to limit the current flowing through the diode when it is forward biased.

DESIGN

The series resistance used for current limiting

$$R = \sqrt{R_f * R_r}$$

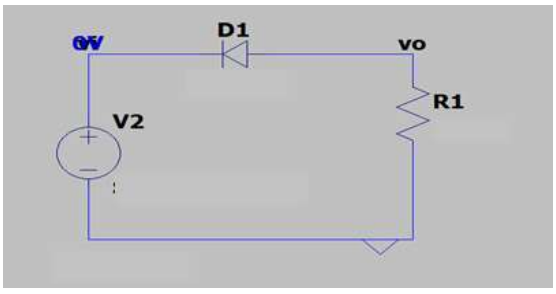
Typical values of forward resistance R_f = 30 Ω and of R_r= 300 kΩ.

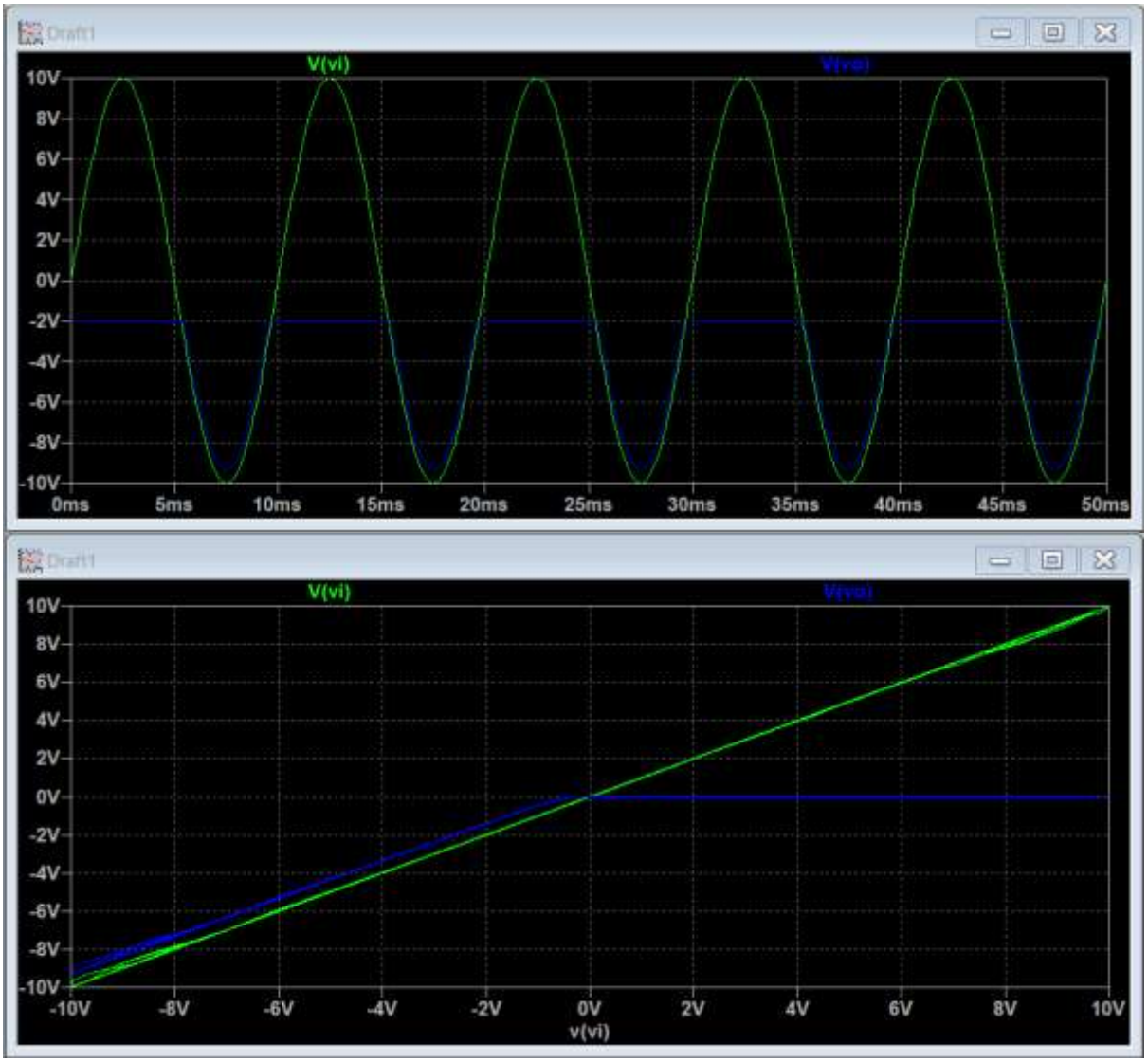
R = $\sqrt{(30 \times 300k)}$ = 3k .Use 3.3 kΩ standard .

SIMULATION RESULTS

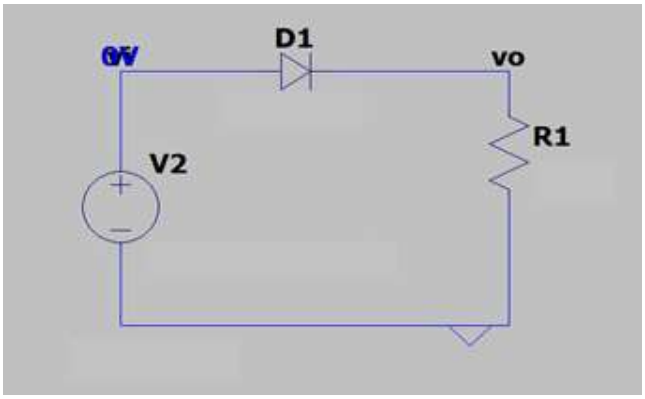
I. Series Clippers

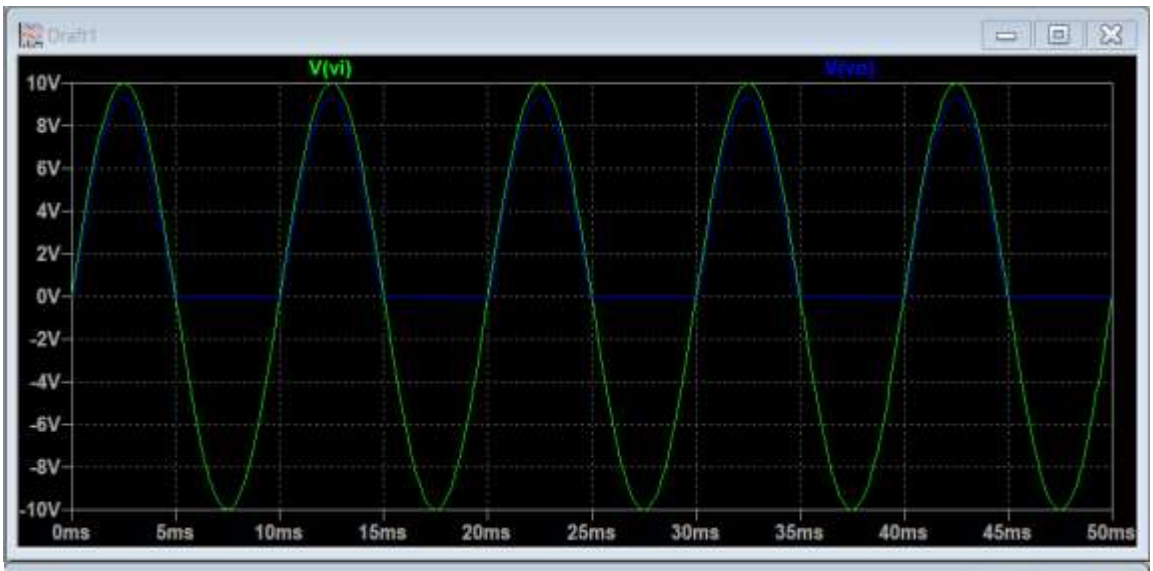
a. Unbiased positive clipper





b. Unbiased negative clipper




Draft1
V(vi)
V(vo)
10V
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
-10V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms


Draft1
V(vi)
V(vo)
10V
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
-10V
-10V
-8V
-6V
-4V
-2V
0V
2V
4V
6V
8V
10V
v(vi)

PROGRAM: 1B

CLAMPING CIRCUITS

AIM: To design positive, negative and biased clamper and obtain transient response and transfer function.

COMPONENTS AND EQUIPMENTS REQUIRED

Diodes, Resistors, Capacitors, Voltage source, connecting wires

THEORY

A Clamper Circuit is a circuit that adds a DC level to an AC signal. Actually, the positive and negative peaks of the signals can be placed at desired levels using the clamping circuits. As the DC level gets shifted, a clamper circuit is called as a Level Shifter. Clamper circuits consist of energy storage elements like capacitors. A simple clamper circuit comprises of a capacitor, a diode, a resistor and a dc battery if required.

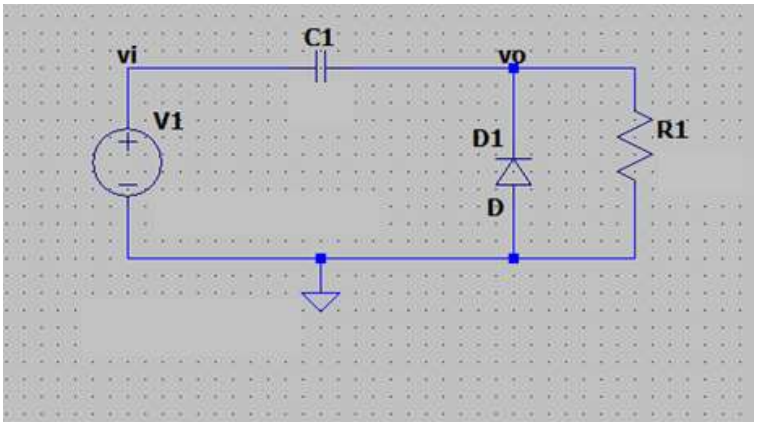
A Clamping circuit restores the DC level. When a negative peak of the signal is raised above to the zero level, then the signal is said to be positively clamped. A Positive Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the positive portion of the input signal.A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. Sometimes an additional shift of DC level is needed. In such cases, biased clampers are used. The working principle of the biased clampers is almost similar to the unbiased clampers.

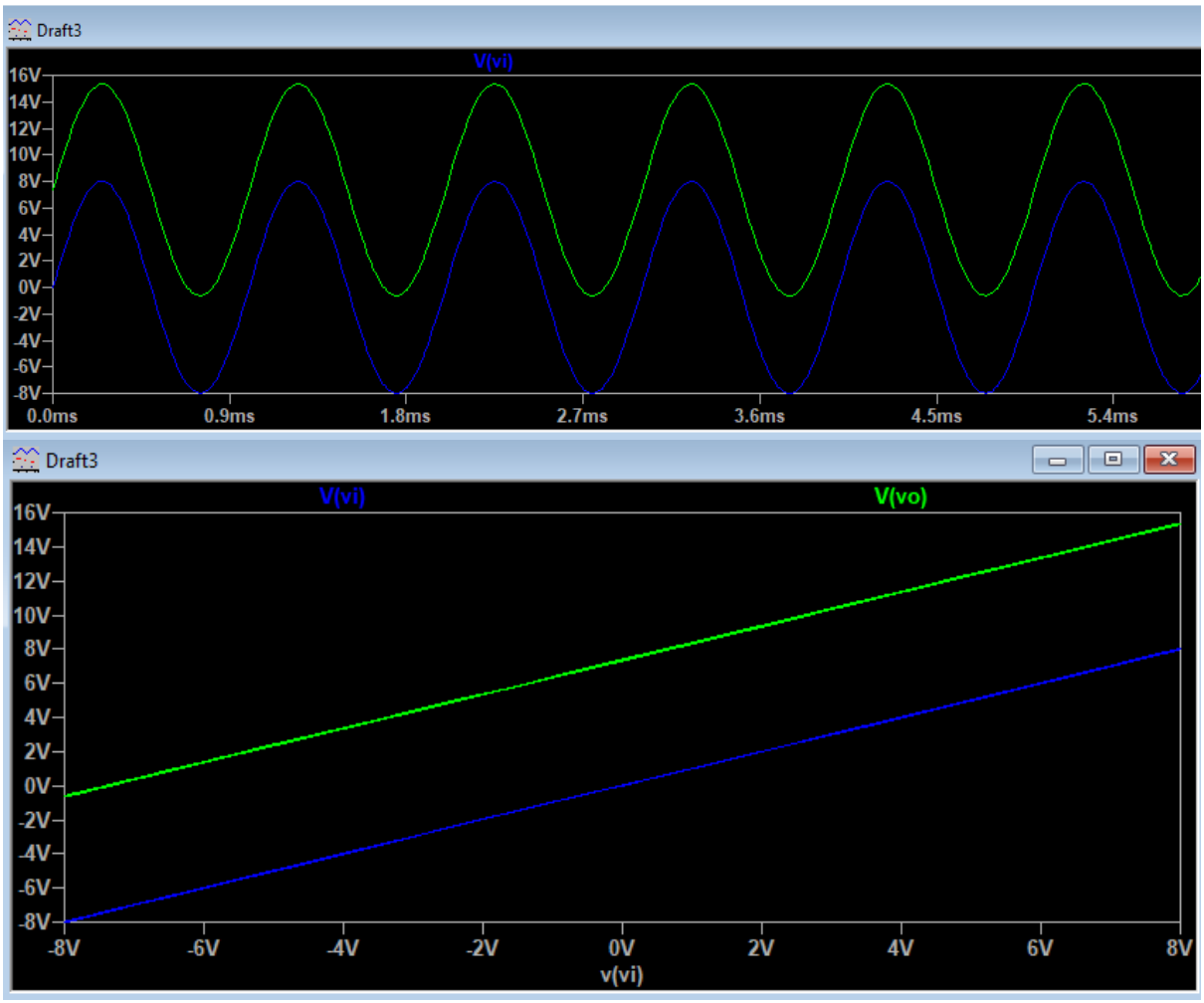
DESIGN

Use suitable value for capacitor C since it has to act like a voltage source.

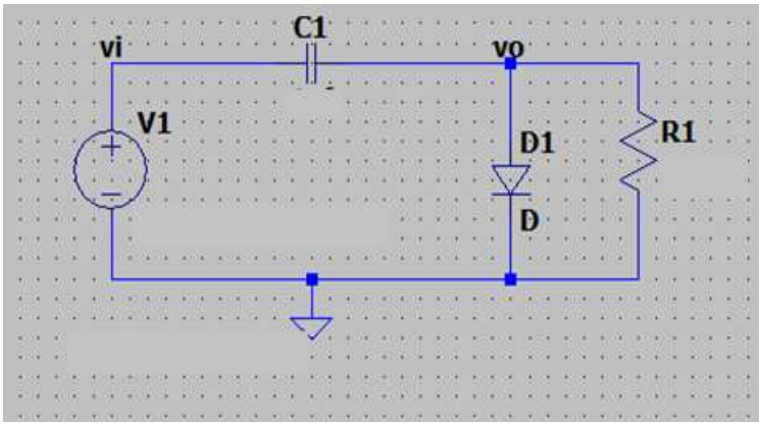
SIMULATION RESULTS

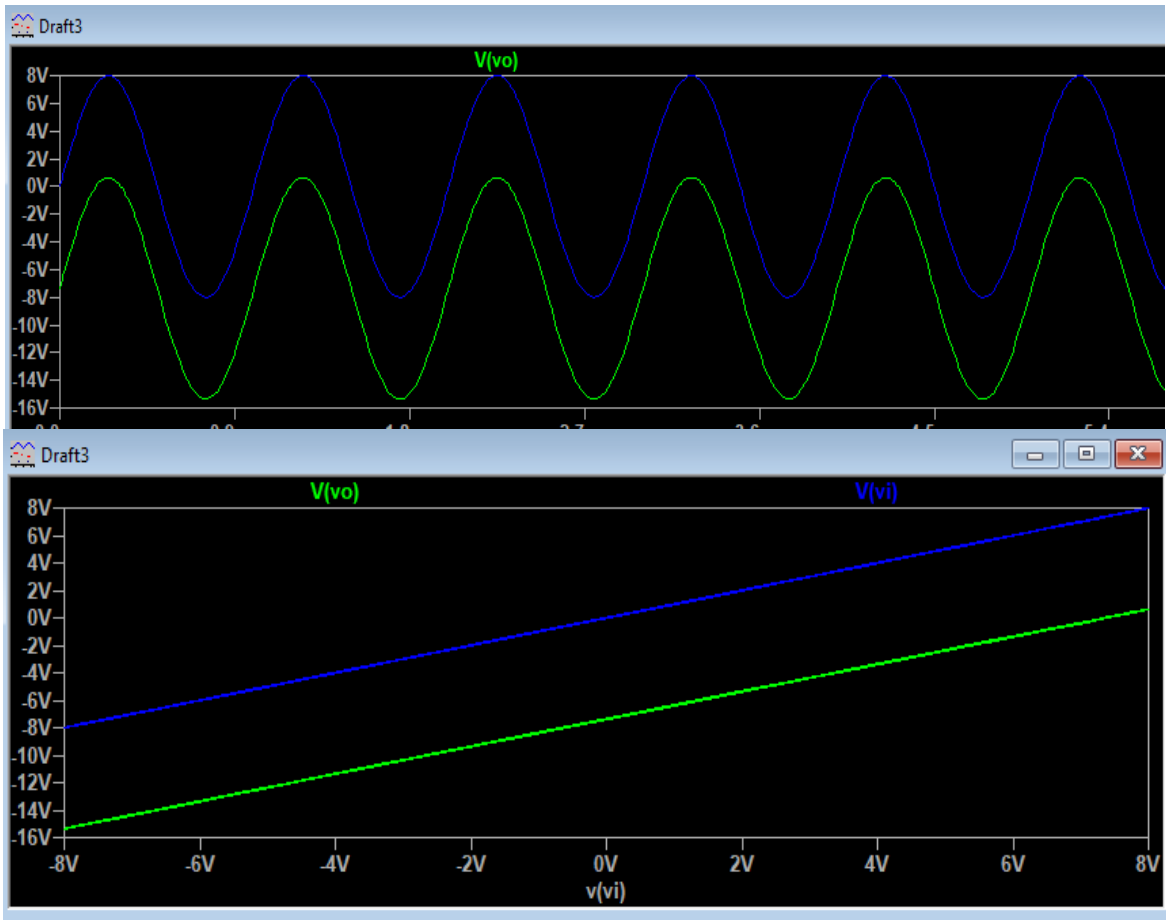
a. Positive camper clamping at 0 V





b. Negative camper clamping at 0 V




Draft3
V(vo)
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
-10V
-12V
-14V
-16V
Draft3
V(vo)
V(vi)
8V
6V
4V
2V
0V
-2V
-4V
-6V
-8V
-10V
-12V
-14V
-16V
-8V
-6V
-4V
-2V
0V
2V
4V
6V
8V
v(vi)

PROGRAM No: 2A

RC DIFFERENTIATOR

AIM: To design an RC differentiator circuit and obtain frequency response

COMPONENTS & EQUIPMENTS REQUIRED

Resistors, capacitors, function generator, connecting wires

THEORY

An RC differentiator circuit is constituted with a capacitor connected in series anda resistor connected in parallel to the output. The time constant RC of the circuit is very small in comparison with the time period of the input signal. The voltage drop across R will be very small in comparison with the drop across C. The current through the capacitor is $C\ \frac{dV_{in}}{dt}$.

Hence the output is proportional to the derivative of the input. Output voltage across R

For RC<<τ, $V_0 = V_R = RC\ \frac{dV_{in}}{dt}$

Differentiated output is proportional to the rate of change of input. When the inputrises to maximum value, differentiated output follows it because the sudden change of voltage is transferred to the output by the capacitor. Since the rate of change of voltage is positive ,differentiated output is also positive. When input remains maximum for a period of time, the rate of change of voltage is zero. So output falls to zero. During this time, input acts like a dc voltage and capacitor offers high impedance to it. So the charges in capacitor drains to earth through the resistance. When input falls to zero, rate of change of input voltage is negative. Then the output also goes to negative.

For the circuit to work as a good differentiator $\theta=90^0$. As $\tan\theta=1/\omega RC$; tan90=infinity. This result can be obtained only if R=0 or C=0, which is practically impossible. Therefore, a reasonable criterion for good differentiation is $\theta=89.4^0$ if $\frac{1}{\omega RC}$=100. So RC=0.0016T will give will give the differentiating practically. Assume RC=0.01T for getting good spike waveforms. The peak of the output of the differentiator gets doubled when the square wave is fed to the input.

DESIGN

RC Differentiator

Case 1: RC<<T

To avoid loading, select R=10 times the output impedance of signal generation.

RC=0.01T

Case2: RC=T

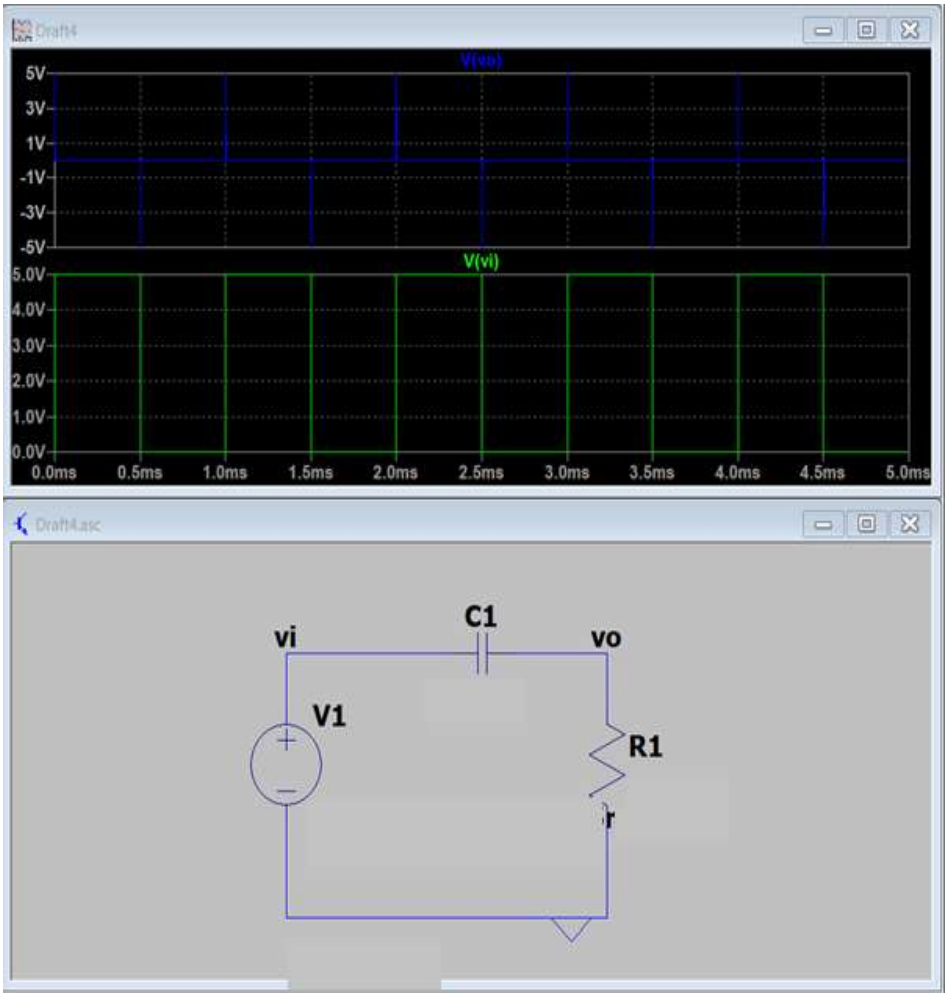
Case3:RC>>T

RC=5T

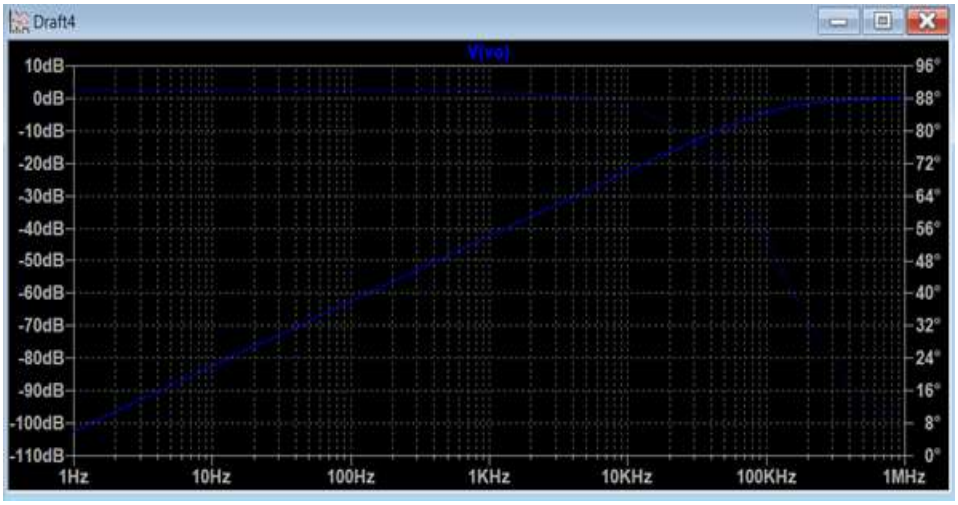
Calculate capacitor value C as per given in the above three cases

SIMULATION RESULTS

1. Output of the circuit for a square wave input



2. Frequency response



PROGRAM No: 2A

RC INTEGRATOR

AIM: To design an RC integrator circuit and obtain the frequency response.

COMPONENTS & EQUIPMENTS REQUIRED

Resistors, capacitors, function generator, connecting wires

THEORY

An RC integrator is constituted by a resistance in series and a capacitor parallel with the output. This circuit produces an output voltage that is proportional to the integralof the input. Here the time constant is very large in comparison with the time required forthe input signal to change. Under this condition the voltage drop across C will be very small in comparison with the drop across R. The current is V_{in}/R since almost all current appears across R. Output voltage across C is

For RC>>τ, $V_C = V_0 = \frac{1}{RC}\int_0^{\tau} V_{in}dt$

Voltage drop across C increases as time increases. A square waveform has positive and negative excursions with respect to its reference zero. If the input is square wave, capacitor charges and discharges from negative voltage to the positive voltage and back.For the circuit to work as a good integrator $\theta=90^0$. As $\tan\theta=\omega RC$; tan90=infinity, which is practically impossible. Therefore a reasonable criterion for good integration is $\theta=89.4^0$ if $\theta=89.4^0$, $\omega RC=95.48^0$. So RC>16T will give the integrating practically.

DESIGN

RC Integrator

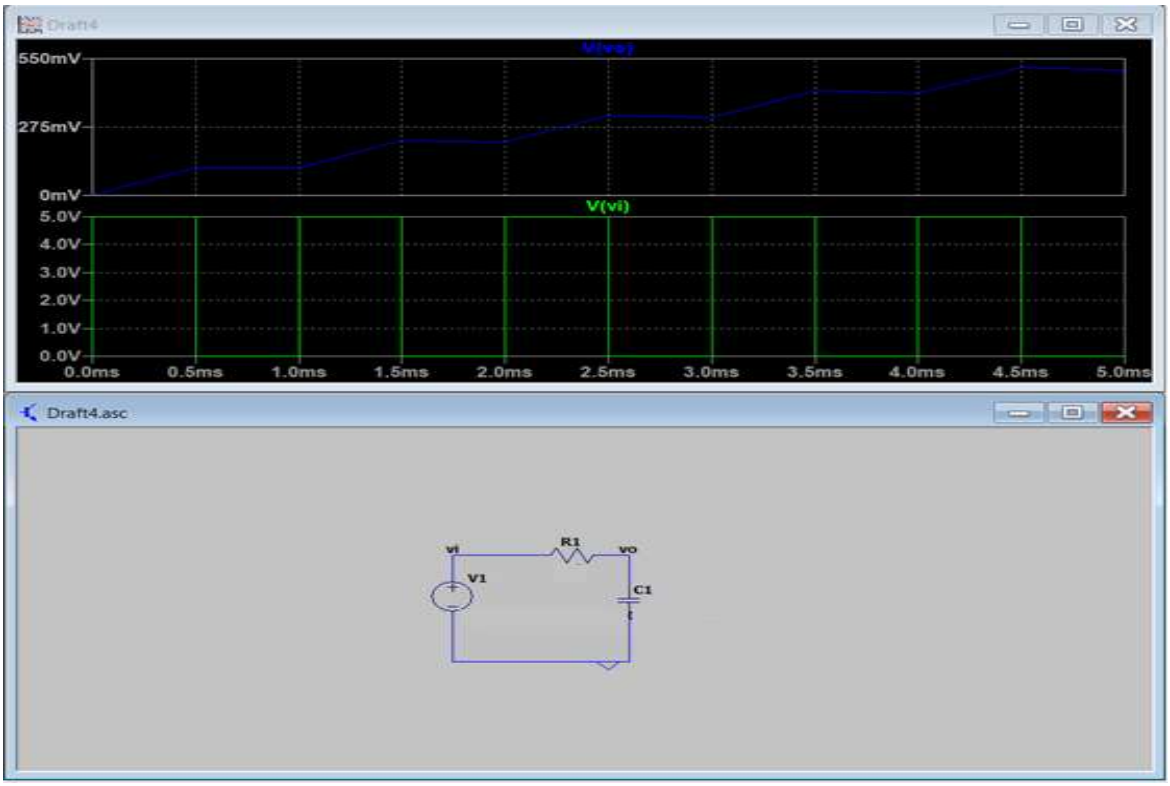
Case 1: RC>>T
To avoid loading, as a general assumption select R=10 times the output impedance of signal generation.

RC=10T

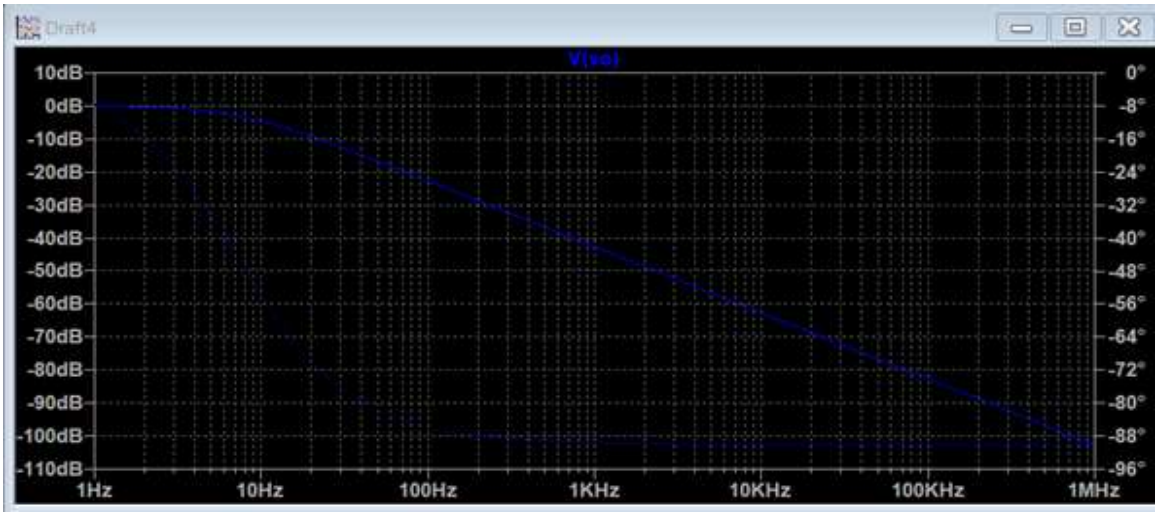
Case2: RC=T
Case3: RC<<T
RC=0.1T. Calculate capacitor value C as per given in the above three cases

SIMULATION RESULTS

1. **Output of the circuit for a square wave input**



2. **Frequency response**



PROGRAM No: 3

RC COUPLED AMPLIFIER

AIM: To verify the characteristics of RC coupled common emitter amplifier for gain A_V.

COMPONENTS & EQUIPMENTS REQUIRED

Resistors, capacitors, transistor, power supply, function generator, connecting wires

THEORY

RC-coupled CE amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter-base junction must be forward biased and the collector base junction must be reverse biased for the proper functioning of an amplifier. In the circuit diagram, an NPN transistor is connected as a common emitter ac amplifier. R_1 and R_2 are employed for the voltage divider bias of the transistor. Voltage divider bias provides good stabilisation independent of the variations of β. The input signal V_{in} is coupled through C_{C1} to the base and output voltage is coupled from collector through the capacitor C_{C2}. The input impedance of the amplifier isexpressed as Zin = $R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{FE}$ re)) and output impedance as $Z_{out} = R_C \backslash\backslash R_L$ where $r_e$is the internal emitter resistance of the transistor given by the expression = 25 mV/I_E, where 25 mV is temperature equivalent voltage at room temperature.

Selection of transistor: Transistor is selected according to the frequency ofoperation, and power requirements. Low frequency gain of a BJT amplifier is given by the expression. Voltage gain $A_v = -h_{FE}RL/ Ri$. In the worst case with $R_L = R_i$; $A_V = -h_{F\ E}.h_{FE}$ of any transistor will vary in large ranges, for BC107 (an AF driver) varies from 100 to 500. Therefore a transistor must be selected such that its minimum guaranteed h_{FE} is greater than or equal to A_V required.

Selection of supply voltage :V_{CC} For a distortion less output from an audio amplifier, the operating point must be kept at the middle of the load line selecting V_{CEQ} = 50% V_{CC} (= 0:5V_{CC}). This means that the output voltage swing in either positive or negative direction is half of V_{CC} . However, V_{CC} is selected 20% more than the required voltage swing. For example, if the required output swing is 10 V, V_{CC} is selected 12 V.

Selection of collector current I_C: The nominal value of I_C can be selected from the data sheet. Usually it will be given corresponding to h_{FE} bias. It is the bias current at which h_{FE} is measured. For BC107 it is 2mA, for SL100 it is 150mA, and for power transistor 2N3055 it is 4 A.

Design of emitter resistor R_E: Current series feedback is used in this circuitusing R_E. It stabilizes the operating point against temperature variation. Voltage acrossR_E must be as high as possible. But, higher drop across R_E will reduce the output voltage swing. So, as a rule of thumb, 10% of V_{CC} is fixed across R_E.

Design of R_C: Value of R_C can be obtained from the relation $R_C = 0.4V_{CC}/I_C$. since remaining 40% of V_{CC} is dropped across R_C.

Design of potential divider R_1 and R_2: Value of I_B is obtained by using the expression $I_B = I_C/h_{FEmin}$. At least $10I_B$ should be allowed to flow through R_1 and $9I_B$ through R_2 for the better stability of bias voltages. If the current through R_1 and R_2 is nearto I_B, slight variation in I_B will a affect the voltage across R_1 and R_2. In other words, the base current will load the voltage divider. When I_B gets branched into the base oftransistor, $9I_B$ flows through R_2. Values of R_1 and R_2 can be calculated from the dc potentials created by the respective currents.

Design of bypass capacitor C_E: The purpose of the bypass capacitor is to bypass signal current to ground. To bypass the frequency of interest, reactance of the capacitor X_{CE} computed at that frequency should be much less than the emitter resistance. As a rule of thumb, it is taken $X_{CE} \leq R_E/10$.

Design of coupling capacitor C_C: The purpose of the coupling capacitor is to couple the ac signal to the input of the amplifier and block dc. It also determines the lowest frequency that to be amplified. Value of the coupling capacitor C_C is obtained such that its reactance X_C at the lowest frequency (say 100 Hz or so for an audio amplifier $\leq$ Rin/10. Here $Rin = R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}\ re)$ where re is the internal emitter resistance of the transistor given by the expression $re = 25\ mV/I_E$ at room temperature.

DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = -h_{FE}\ R_L/\ Rin$ where $Rin = R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}\ re)$

DC biasing conditions:

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,

V_{RC} = 40% of V_{CC}

V_{RE} = 10% of V_{CC}

V_{CE} = 50% of V_{CC}

Design of Rc:

$V_{RC} = Ic\ Rc$

Design of R_E:

$V_{RE} = I_E\ R_E$

Design of potential divider R_1 and R_2:

$I_B = I_C/\ h_{FE}$

With general assumptions take the current through R_1 as **10**I_B and that through R_2 as **9**I_B to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across R_2= V_{BE}+V_{RE}= 9 I_B R_2

V_{R1}= Voltage across R_1= Vcc-V_{R2} =10 I_B R_1

Design for R_1 and R_2 from the above two equations

Design of R_L:

Gain of the common emitter amplifier is given by the expression A_V = -(rc/re). Where rc = R_C\\R_L and re = 25 mV/I_C.

From the above relations, we get R_L = - A_V (R_C re)/ (R_C + re A_V)

Design of coupling capacitor Cc_1 and Cc_2:

X_{C1} should be less than the input impedance of the transistor. Here, Rin is the input impedance.

With general assumption,
$X_{C1} \leq$ Rin /10.
where Rin = R_1\\R_2\\ (1 + h_{FE} re)
i.e. $Cc_1 \leq$ Rin/2π *f_L*10, where f_L is the lower cut-off frequency

Similarly, $X_{C2} \leq$Rout/10, where Rout = R_C
$Cc_2 \leq$ Rout/2π *f_L*10

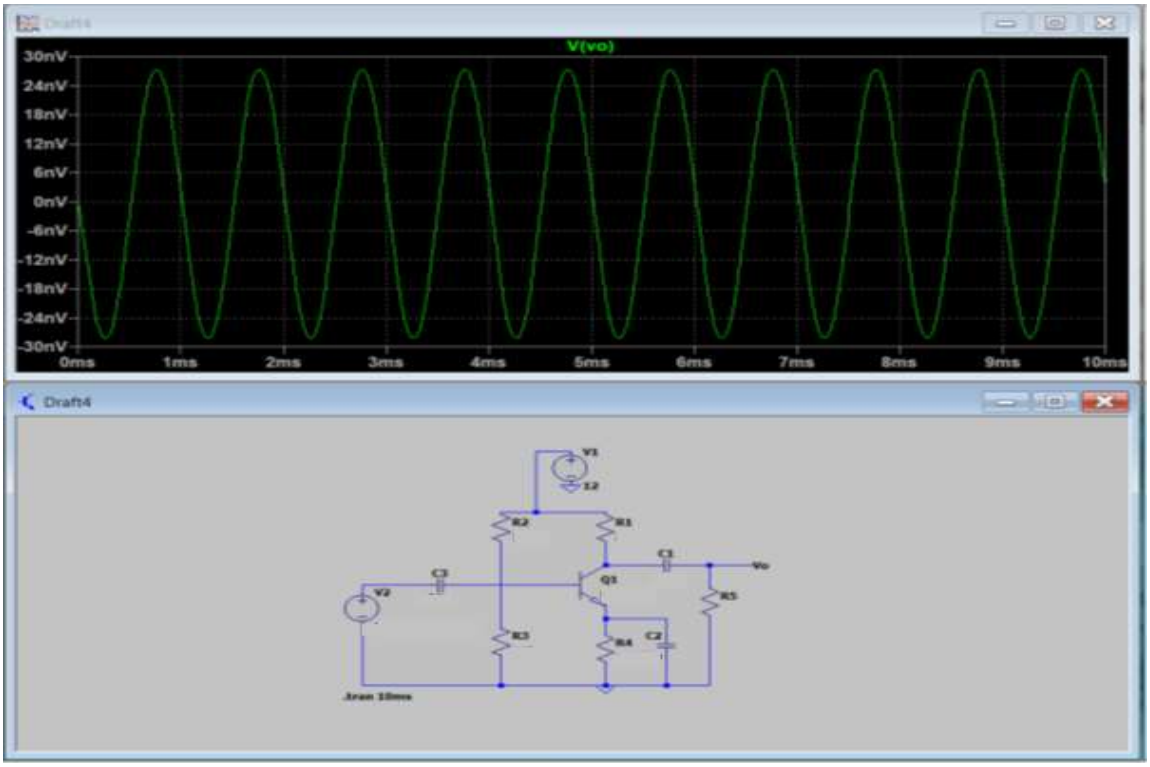
Design of bypass capacitor C_E:

To bypass the lowest frequency, say f_{lo}, X_{CE} should be less than or equal to R_E
i.e., $X_{CE} \leq R_E$/ 10
$C_E \leq R_E$/2π * f_{lo}*10

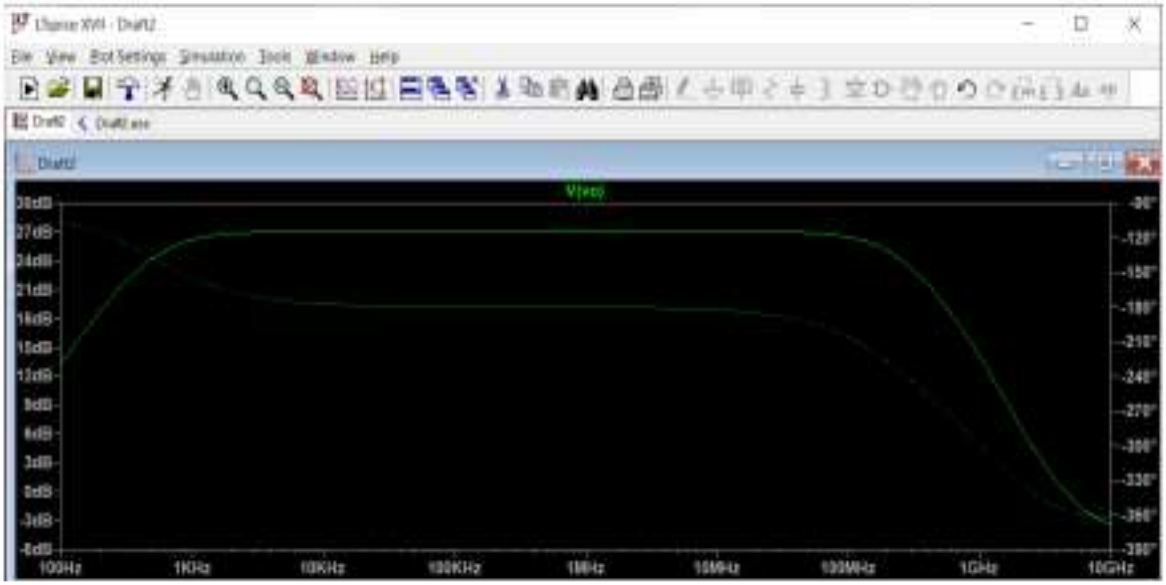
Circuit parameters	Design equations
R_1	(Vcc- V_{BE} -V_{RE}) h_{fe} / 10 Ic
R_2	(V_{BE}+V_{RE}) h_{fe} / 9 Ic
R_C	V_{RC} / I_C
R_E	V_{RE} / I_E
R_L	- A_V (R_C re)/ (R_C + re A_V)
C_{C1}	$\leq$ (R_1\\ R_2\\(1+h_{fe} re))/2π * f_L*10
C_{C2}	$\leq$ R_C/2π * f_L*10
C_E	$\leq$ R_E/2π * f_{lo}*10

SIMULATION RESULTS

1. Output signal



2. Frequency response



PROGRAM No:4

COMMON SOURCE AMPILFIER

AIM: To verify the characteristics of common source amplifier for a voltage gain of A_V

COMPONENTS & EQUIPMENTS REQUIRED

Resistors, capacitors, transistor, power supply, function generator, connecting wires

THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P -N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate.

DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = gm(R_D \backslash\backslash R_L)$ where gm =transconductance

DC biasing conditions:

Voltage V_{GS} and current I_D are transistor dependent

With general assumptions,

$V_{RD} = V_{DS}$ =45% of V_{CC}

V_{RS}= 20% of V_{CC}

Design of R_D:

$V_{RD} = I_D R_D$

Design of R_S:

$V_{RS} = I_S R_S$, $I_S = I_D$ as current through gate is zero

Design of potential divider R_1 and R_2:

V_{R2}= Voltage across R_2= V_{GS}+V_{RS}= V_{DD}*(R_2/ R_1+ R_2)

Design R_2 from the above equation.

R_1 value should be large to ensure zero gate current.

Design of R_L:

Gain of the common source amplifier is given by the expression $A_V = gm(R_D \backslash\backslash R_L)$

i.e. $R_L = (gmR_D - A_V)/ R_D A_V$

Design of coupling capacitor Cc_1 and Cc_2:

X_{C1} should be less than the input impedance of the transistor. Here, gate impedance R_G is the input impedance.

With general assumption,
$X_{C1} \leq R_G /10$, R_G is in M Ω range
i.e., $Cc_1 \leq R_G / 2\pi * f_L * 10$, where f_L is the lower cut-off frequency

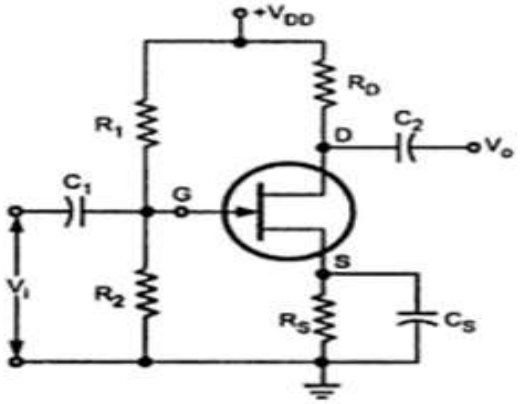
Similarly, $X_{C2} \leq R_D /10$, where
$Cc_2 \leq R_D /2\pi * f_L * 10$

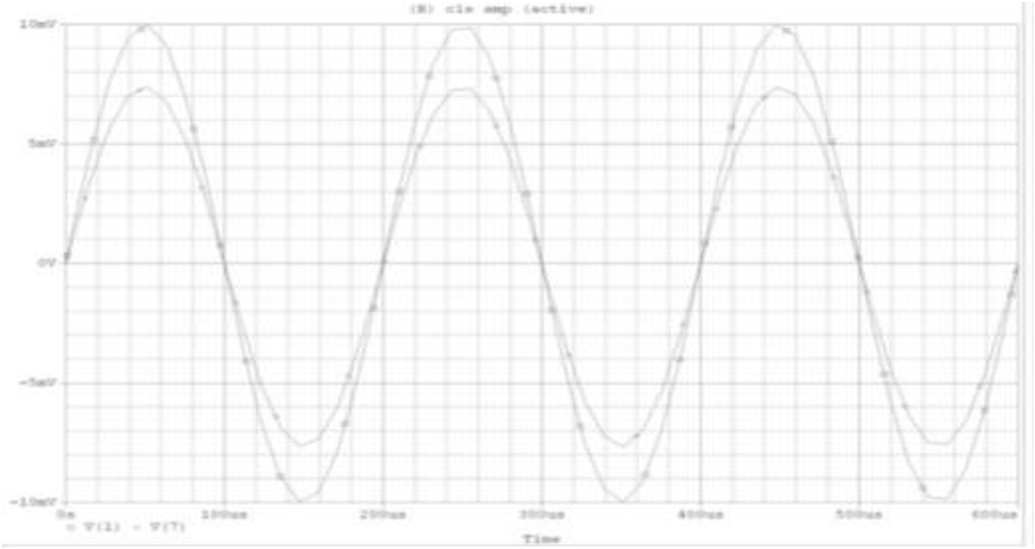
Design of bypass capacitor C_S:

To bypass the lowest frequency, say f_{lo}, X_{CS} should be less than or equal to R_E
i.e., $X_{CS} \leq R_S/ 10$
$C_S \leq R_S/2\pi * f_{lo} * 10$

Circuit parameters	Design equations
R_1	M Ω range
R_2	$R_1/((V_{DD}/(V_{GS}+V_{RS}))-1)$
R_D	V_{RD} / I_D
R_S	V_{RS} / I_D
R_L	$(gmR_D - A_V)/ R_D A_V$
C_{C1}	$\leq R_G /(2\pi * f_L * 10)$
C_{C2}	$\leq R_D/2\pi * f_L * 10$
C_E	$\leq R_S/(2\pi * f_{lo} * 10)$

SIMULATION RESULT





PROGRAM No:5

RC PHASE SHIFT OSCILLATOR

AIM: To design an RC phase shift oscillator using BJT for a frequency f and observe the output waveform.

COMPONENTS & EQUIPMENTS REQUIRED

Resistors, capacitors, transistor, power supply, function generator, connecting wires

THEORY

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is A β= 1 where A is the gain of the amplifier and β is the feedback factor. The unity gain means signal is in phase. (If the signal is 180 out of phase, gain will be 1.) If a common emitter amplifier is used, with a resistive collector load, there is a 180 phase shift between the voltages at the base and the collector. Feedback network between the collector and the base must introduce an additional 180^0 phase shift at a particular frequency.

In the figure shown, three sections of phase shift networks are used so that each section introduces approximately 60 phase shift at resonant frequency. By analysis, resonant frequency f can be expressed by the equation,

$$f = \frac{1}{2\pi RC\sqrt{(6 + 4(R_C/R))}}$$

The three section RC network offers a β of 1/29. Hence the gain of the amplifier should be 29. For this, the requirement on the h_{FE} of the transistor is found to be

$$h_{FE} \geq 23 + 29(R/R_C) + 4(R_C/R)$$

The phase shift oscillator is particularly useful in the audio frequency range.

DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = -h_{FE}\, R_L / Rin$ where $Rin = R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}\, re)$

DC biasing conditions:

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,
V_{RC} = 40% of V_{CC}
V_{RE} = 10% of V_{CC}
V_{CE} = 50% of V_{CC}

Design of Rc:
V_{RC}= Ic Rc

Design of R_E:
V_{RE}= I_E R_E

Design of potential divider R_1 and R_2:

I_B= I_C/ h_{FE}
With general assumptions take the current through R_1 as **10**I_B and that through R_2 as **9**I_B to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across R_2= V_{BE}+V_{RE}= 9 I_B R_2

V_{R1}= Voltage across R_1= Vcc-V_{R2} =10 I_B R_1

Design for R_1 and R_2 from the above two equations

Design of R_L:

Gain of the common emitter amplifier is given by the expression A_V = -(rc/re). Where rc = R_C\\R_L and re = 25 mV/I_C.

From the above relations, we get R_L = - A_V (R_C re)/ (R_C + re A_V)

Design of coupling capacitor Cc_1 and Cc_2:

X_{C1} should be less than the input impedance of the transistor. Here, Rin is the input impedance.

With general assumption,
$X_{C1} \leq$ Rin /10. where Rin = R_1\\R_2\\ (1 + h_{FE} re)
i.e. $Cc_1 \leq$ Rin/2π *f_L*10, where f_L is the lower cut-off frequency

Similarly, $X_{C2} \leq$Rout/10, where Rout = R_C
$C_{C2} \leq$ Rout/2π *f_L*10

Design of bypass capacitor C_E:

To bypass the lowest frequency, say f_{lo}, X_{CE} should be less than or equal to R_E
i.e., $X_{CE} \leq R_E$/ 10
$C_E \leq R_E$/2π * f_{lo}*10

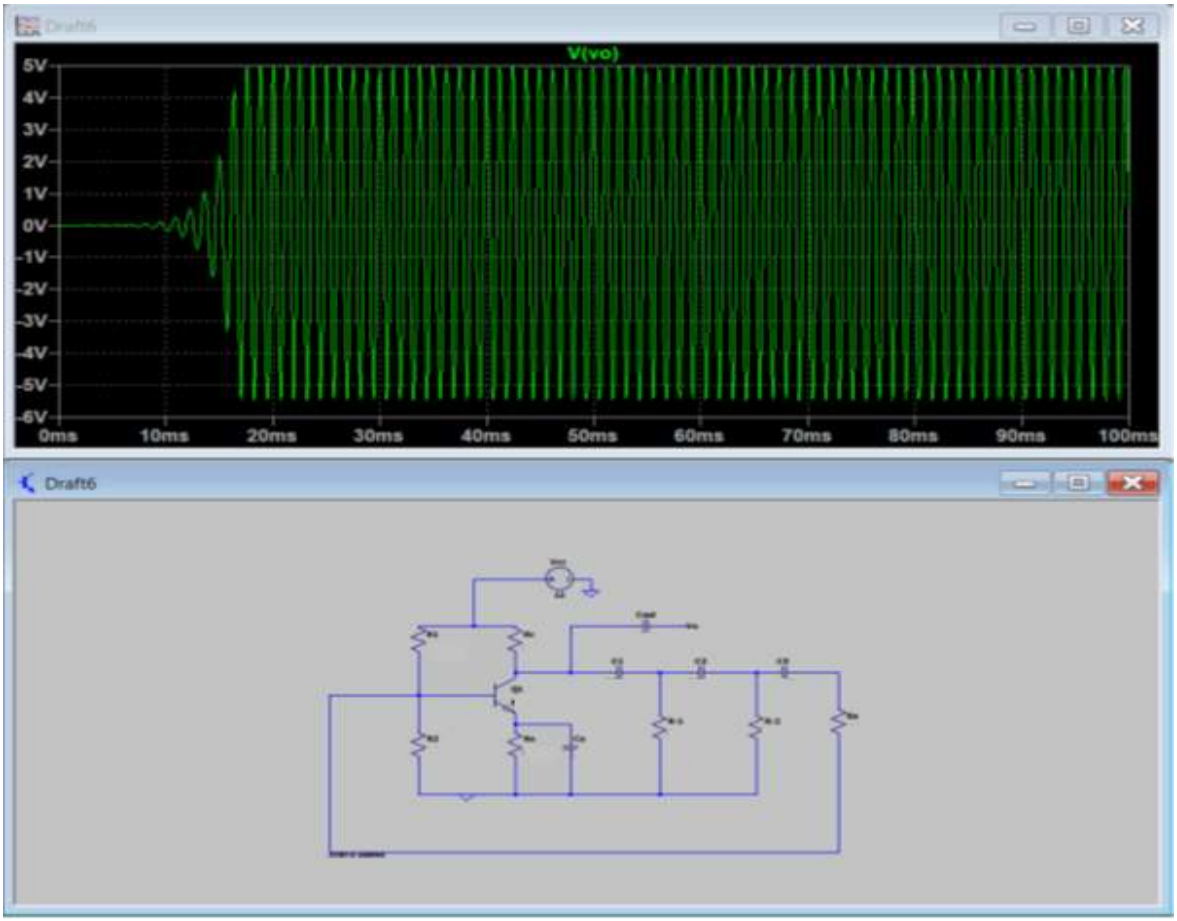
Design of frequency selective network:

$f = 1 / (2\pi RC \sqrt{(6 + 4 Rc/R)})$

The frequency determined by R and Rc must be selected in such a way to avoid loadingof amplifier. So, R is taken as 2Rc. From the value of R calculate C.

Circuit parameters	Design equations
R_1	$(Vcc- V_{BE} -V_{RE}) h_{fe} / 10 Ic$
R_2	$(V_{BE}+V_{RE}) h_{fe} / 9 Ic$
R_C	V_{RC} / I_C
R_E	V_{RE} / I_E
R_L	$- A_V (R_C re)/ (R_C + re A_V)$
C_{C1}	$\leq (R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{fe} re))/2\pi * f_L*10$
C_{C2}	$\leq R_C/2\pi * f_L*10$
C_E	$\leq R_E/2\pi * f_{lo}*10$
f	$1 / (2\pi RC \sqrt{(6 + 4 Rc/R)})$

SIMULATION RESULTS



PROGRAM No:6

CASCADE AMPLIFIER

AIM: To design a cascade amplifier for a gain of A_V and obtain the transient response and frequency response.

COMPONENTS REQUIRED

Transistors, Resistors, Capacitors, Voltage source, connecting wires

THEORY

A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times, the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker.

DESIGN

Output requirements: Mid-band voltage gain of the amplifier = A_V

$A_V = A_{V1} * A_{V2}$ where A_{V1} and A_{V2} are voltage gain of first stage and second stage respectively.
A_{V1} should be larger than A_{V1} to avoid high input voltage to second stage.

$A_{V1} = (R_C \backslash\backslash R_{in2})/(re+R_{e1})$ where $re = 25\ mV/I_C$ and $R_{e1} = R_E - R_e{}^1$
and $R_{in2} = R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{fe}\, re)$
and $A_{V2} = (Rc \backslash\backslash R_L)/re$

DC biasing conditions:

Value of collector current I_C is transistor dependent. Assume suitable value for supply Vcc

With general assumptions,
V_{RC} = 40% of V_{CC}
V_{RE} = 10% of V_{CC}
V_{CE} = 50% of V_{CC}

Design of R_{C1} and R_{C2}:

$V_{RC} = Ic\ Rc$
Choose Rc1= Rc2

Design of potential divider R_1 and R_2:

$I_B = I_C / h_{FE}$
With general assumptions take the current through R_1 as $\mathbf{10}I_B$ and that through R_2 as $\mathbf{9}I_B$ to avoid loading potentialdivider by the base current.

V_{R2}= Voltage across $R_2 = V_{BE} + V_{RE} = 9\ I_B\ R_2$

V_{R1}= Voltage across $R_1 = Vcc - V_{R2} = 10\ I_B\ R_1$

Design for R_1 and R_2 from the above two equations
Choose $R_{11} = R_{21}$ and $R_{12} = R_{22}$

Design of R_{E1} and R_{E2}

R_{E1} of first stage is split into R_e and R_e^1
$V_{RE1} = I_E\ R_{E1} = I_C\ R_{E1}$
Find R_{E1} from above relation. Choose $R_{E1} = R_{E2}$
$A_{V1} = (R_C \backslash\backslash R_{in2})/(re + R_{e1})$
Substituting for A_{V1}, R_C, R_{in2}, re the value for R_{e1} can be calculated.
Then from equation $R_{e1} = R_E - R_e^1$, value for R_e^1 can be calculated.

Design of R_L:

Gain of second stage $A_{V2} = (Rc \backslash\backslash R_L)/re$

From the above relations, we get $R_L = (R_C - A_{V2}\ re)/ (R_C\ re\ A_{V2})$

Design of coupling capacitor Cc_1, Cc_2 and Cc_3:

X_{C1} should be less than the input impedance of the transistor. Here, Rin is the input impedance.
With general assumption,
$X_{C1} \leq Rin/10$.
where $Rin = R_1 \backslash\backslash R_2 \backslash\backslash (1 + h_{FE}\ re)$
i.e., $Cc_1 \leq Rin/2\pi * f_L * 10$, where f_L is the lower cut-off frequency
Choose $Cc_1 = Cc_2$

Similarly, $X_{C3} \leq Rout/10$, where $Rout = R_C$
$C_{C3} \leq Rout/2\pi * f_L * 10$

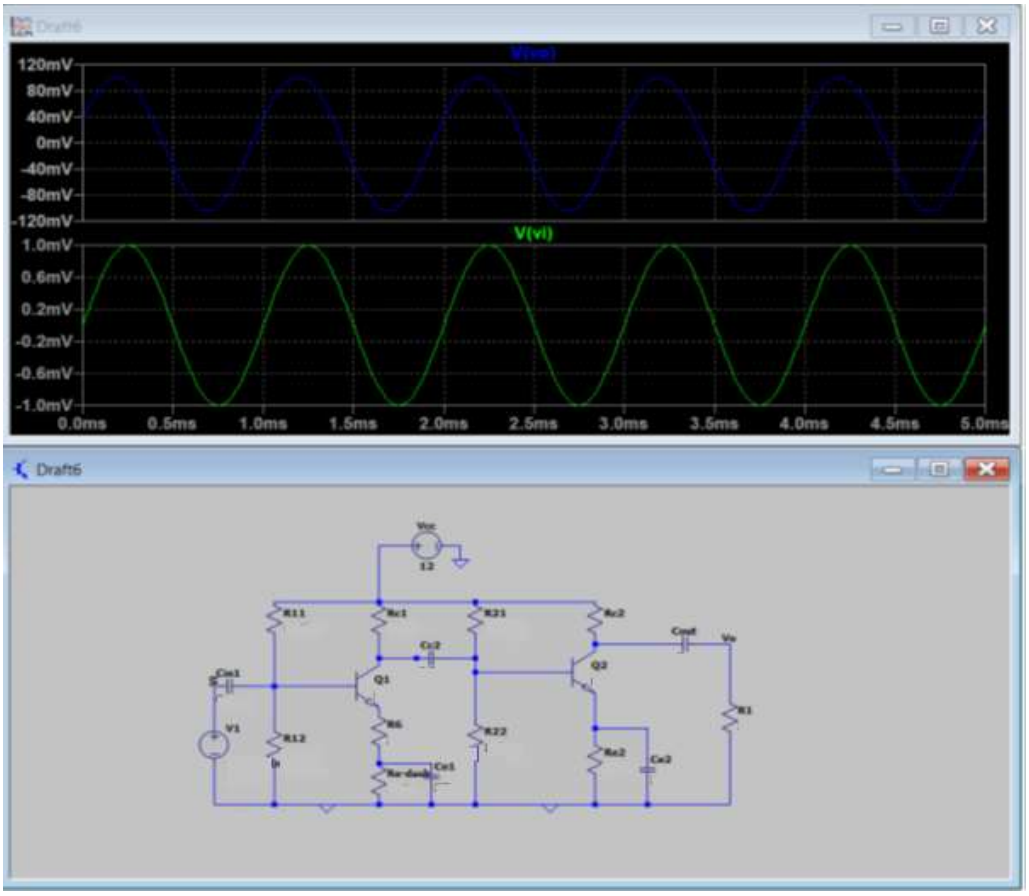
Design of bypass capacitor C_{E1} and C_{E2}:

To bypass the lowest frequency, say f_{lo}, X_{CE} should be less than or equal to R_E
i.e., $X_{CE} \leq R_E/10$
$C_E \leq R_E/2\pi * f_{lo} * 10$
Choose $C_{E1} = C_{E2}$

Circuit parameters	Design equations
$R_{11} = R_{21}$	$(Vcc- V_{BE} -V_{RE}) h_{fe} / 10 Ic$
$R_{12} = R_{22}$	$(V_{BE}+V_{RE}) h_{fe} / 9 Ic$
$R_{C1}= R_{C2}$	V_{RC} / I_C
$R_{E1} = R_{E2}$	V_{RE} / I_E
R_L	$(R_C -A_{V2} re)/ (R_C re A_{V2})$
$C_{C1} = C_{C2}$	$\leq (R_1 \backslash\backslash R_2 \backslash\backslash (1+h_{fe} re))/2\pi * f_L*10$
C_{C3}	$\leq R_C/2\pi * f_L*10$
$C_{E1} = C_{E2}$	$\leq R_E/2\pi * f_{lo}*10$

SIMULATION RESULTS

1. Output waveform



2. Frequency response