LABORATORY MANUAL

Analog Integrated Circuits & Instrumentation Lab

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COLLEGE OF ENGINEERING

TRIVANDRUM

2021

AEL 331: PART A: Analog Integrated Circuits Lab

Exp No: 01
Date:

Basic circuits using operational amplifiers - inverting amplifier, non-inverting amplifier, integrator.

Aim: To study frequency response of basic operational amplifier circuits.

Components required: Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory: Operational amplifier, in short, op-amp is a versatile device used to amplify AC and DC signals. Though it was originally designed for computing mathematical operations such as addition, multiplication, differentiation, integration etc., it is widely used for variety of applications like oscillators, filters, regulators, clipping circuits, waveform generators etc.

The symbol of op-amp represents a circuit with two input terminals an output terminal and two bias supply points.

The **741 IC:** It is a frequency compensated and short circuit protected IC.741C is its commercial version with operating temperature ranges from 0^0C to $+70^0$C. 741 needs positive and negative dc sources for bias supply connections V^+ and V^-. This is provided by either a dual power supply or two power supplies. When dual power supply is used its positive terminal is connected to the V^+ pin of the IC and the negative terminal is connected to the V^- pin of the IC. The ground terminal of the dual power supply is connected to the ground point of the circuit. When two power supplies are used positive terminal of one supply and negative terminal of the other power supply are connected to the V^+ and V^- pins of the IC respectively.

Inverting Amplifier: This is one of the most popular op-amp circuits. The polarity of the input voltage gets inverted at the output. If a sine wave is fed to the input of this amplifier, the output will be an amplified sine wave with 180^0 phase shift. The gain of the inverting amplifier is given by $A= -R_f/R_i$. where R_f is the feedback resistance and R_i is the input resistance.

Noninverting Amplifier: This circuit provides a gain to the input signal without any change in polarity. The gain of noninverting amplifier is given by $A=1+R_f/R_i$. Input impedance is extremely large.

Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by

$$V_o = -1/R_1C_f \int_o^t V_i \, dt$$

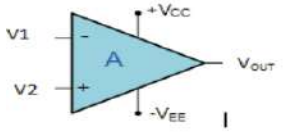
At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.

Comparator: This circuit compares one analogue voltage level with another analogue voltage level, or some pre-set reference voltage, V_{REF} and produces an output signal based on this voltage comparison. The op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.

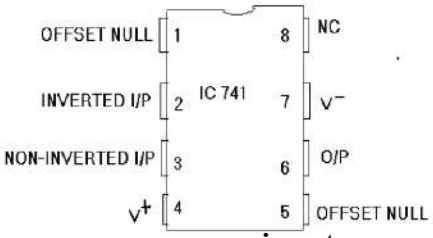
The output saturation voltages are about 2V below the magnitudes of the dc power supply levels. For supply voltages of ($^{+}$-15V),V_{sat} will be approximately ($^{+}$-13V).

Sr. No.	Characteristics	Value for IC 741	Ideal value
1	Input resistance Ri	2 MΩ	∞
2	Output resistance Ro	75 Ω	0
3	Voltage gain Av	2 X 10^5	∞
4	Bandwidth BW	1 MHz	∞
5	CMRR	90 dB	∞
6	Slew rate S	0.5 V/μS	∞
7	Input offset voltage	2 mV	0
8	PSRR	150 μV/V	0
9	Input bias current	50 nA	0
10	Input offset current	6 nA	0

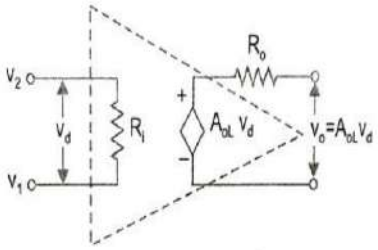
Circuit diagram and waveforms:



op-amp symbol

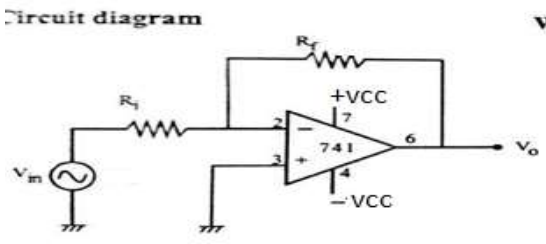


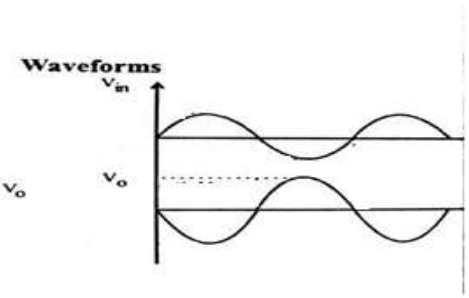
op-amp pin out



equivalent circuit

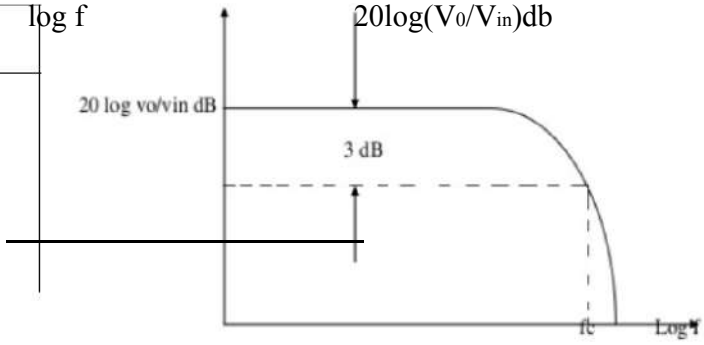
Inverting amplifier





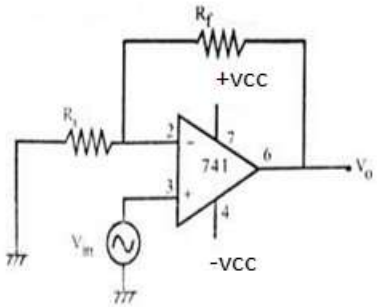
Tabular Column & Frequency Response

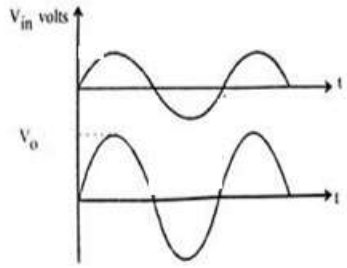
F(Hz)		V_0 (volts)	log f	$20\log(V_0/V_{in})$db

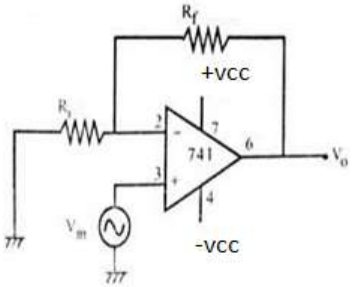


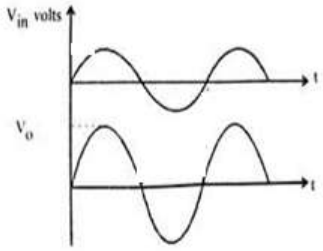
Non inverting amplifier

Circuit Diagram & Waveform









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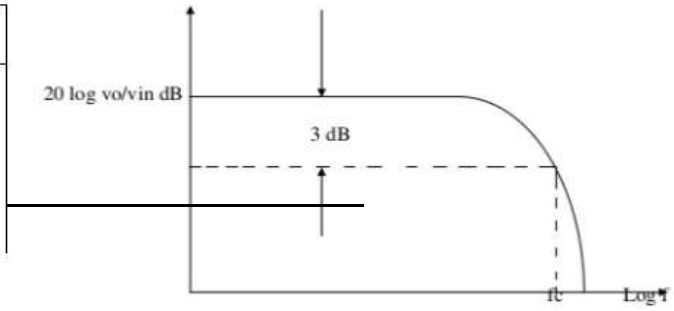
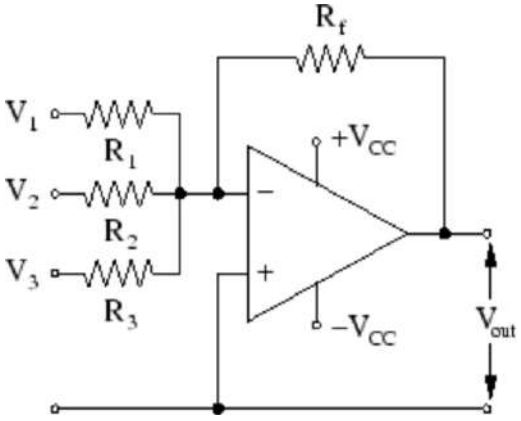
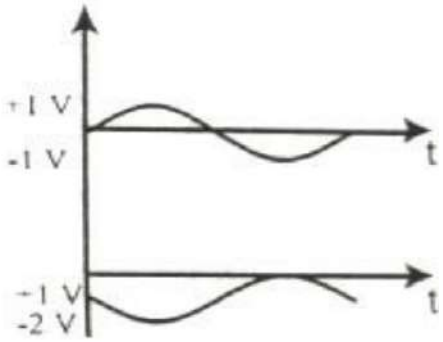


Adder

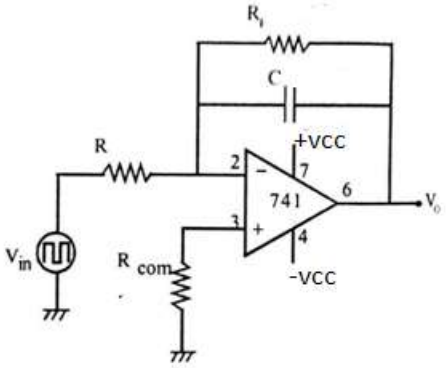
Circuit Diagram & Waveforms

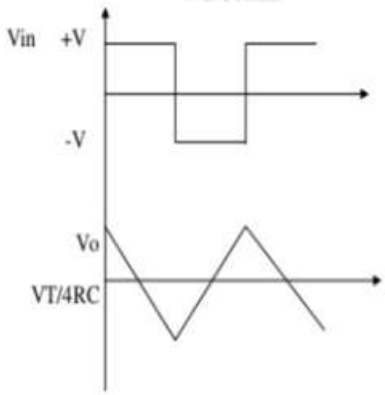




Integrator

Circuit Diagram & Waveforms





Tabular Column & Frequency Response

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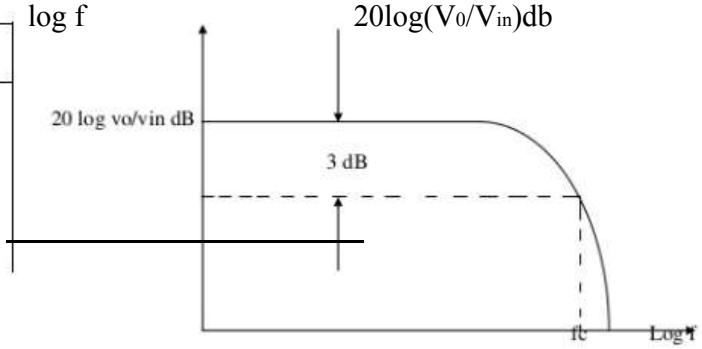
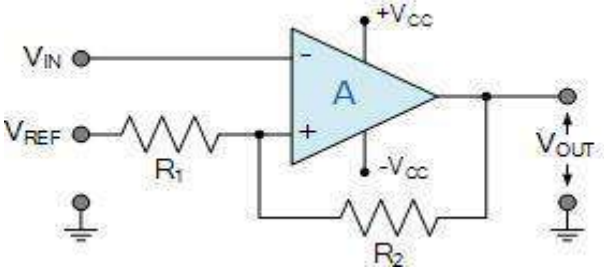
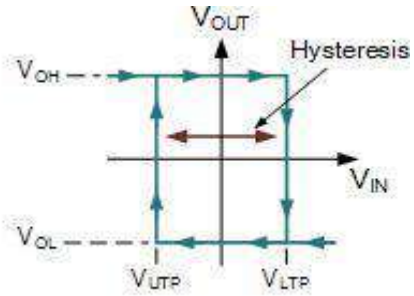


Comparator

Circuit Diagram & Waveforms





Design:

Inverting amplifier:

$A = -Rf/R1$

Take $A = 1$

$Rf = R1$

Non inverting amplifier:

$A = 1 + Rf/R1$

Take $A = 2$

$Rf = R1$

Integrator:

Let input frequency be, f= 1 kHz

$f = 1/ (2\pi RC)$

Take C=0.01 μf. And calculate R.

Select $R_f = 10$ R

Procedure:

I. Inverting amplifier and Non inverting amplifier

1. Set up the inverting amplifier on the bread board.

2. Feed a $2V_{pp}$ sine wave and observe the input and output simultaneously on CRO. Verify whether the output is $22V_{pp}$ sine wave in phase with input.

3. Set up the non inverting amplifier on the bread board.

4. Feed a $2V_{pp}$ sine wave and observe the input and output simultaneously on CRO. Verify whether the output is $20V_{pp}$ sine wave with 180^0 out of phase with input.

II. Integrator

1. Set up the integrator circuit.

2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.

3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response

III. Comparator.

1. Set up the comparator circuit.
2. Feed the inputs and verify the output.

Results: Familiarized with basic operational amplifier integrated circuits.

Exp No: 02
Date:

Difference Amplifier And Instrumentation Amplifier

Aim: To design and setup a difference amplifier and instrumentation amplifier using opamp.

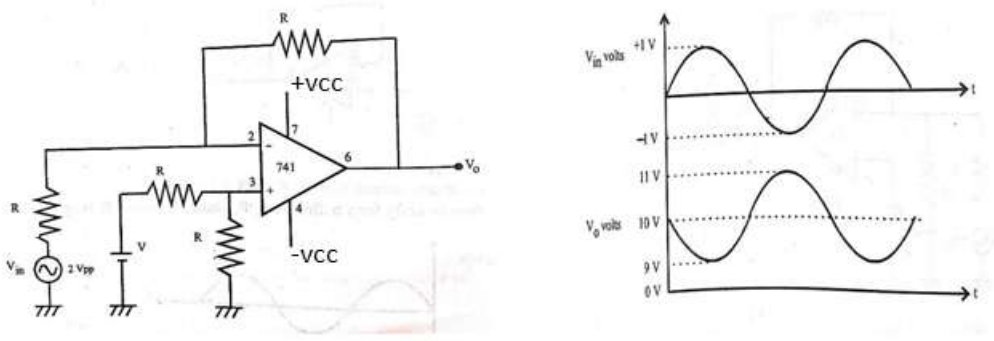
Components required: Op-amp, resistors, capacitors, breadboard, CRO, function generator power supplies.

Theory: The difference amplifier circuit is very useful in detecting very small differences in the signal. since the gain is R_F/R_1 can be selected to be very large. The output $V_O = -R_F/R_1(V2-V1)$.If all the external resistors are of equal value, the gain of the amplifier becomes one. Thus the output is V_2-V_1. Hence the name subtractor.

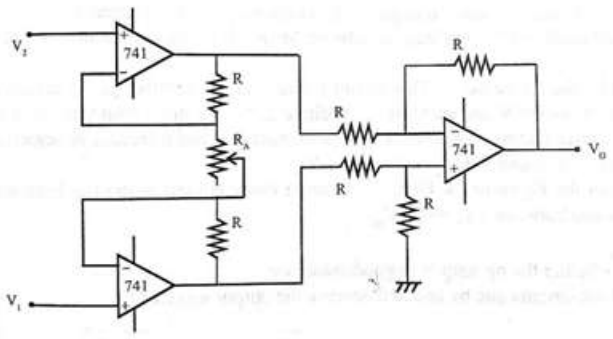
Instrumentation amplifiers are widely used in data acquisition systems, remote sensing applications and instrumentation systems to measure temperature, humidity, light intensity and weight etc. Most of the instrumentation systems use a transducer in a bridge circuit. Instrumentation amplifier facilitates the amplification of potential difference take place due to the imbalance of the bridge circuit proportional to a change in physical quantity. The main feature of instrumentation amplifiers are high gain, high input resistance, high CMRR etc.

Circuit diagram and waveforms:

Difference amplifier



Instrumentation amplifier



Design:

Difference amplifier:

$V_0 = (V_1)/2\ (1+R/R) - V_2\ (R/R)$

$= V_1 - V_2$

Instrumentation amplifier

We have, $V_0=(V_1-V_2)[1+2R/R_A]$

Given, $1+2R/R_A=3$

Assume R and $R_A \cong 10K$. Use 10K pot in series with 470Ω

Procedure:

1.Verify the condition of op-amps.

2.Setup the circuit..

3.verify the output.

Result: Designed the difference and instrumentation amplifier.

Exp No: 03
Date:

Schmitt trigger circuit using op amps

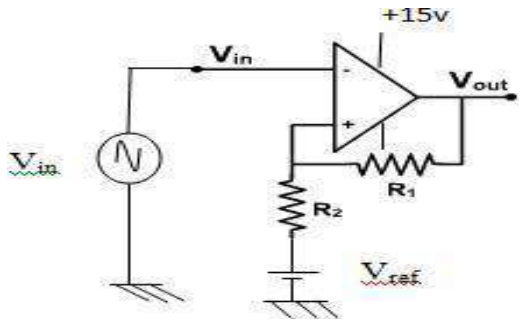
Aim: To design and set up a schmitt trigger circuit using op-amps for various LTP and UTP.

Components required: Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

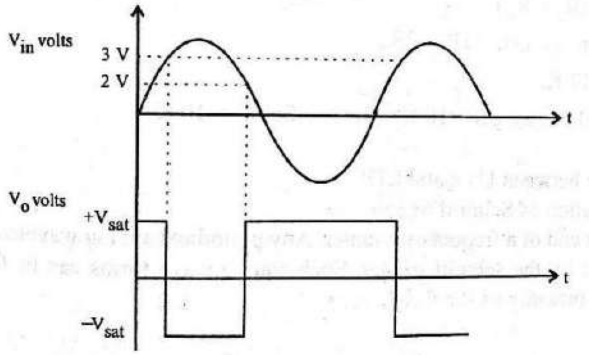
Theory: Schmitt Trigger converts an irregular shaped waveform to a square wave or pulse. Here, the input voltage triggers the output voltage every time it exceeds certain voltage levels called the upper threshold voltage VUTP and lower threshold voltage VLTP. The input voltage is applied to the inverting input. Because the feedback voltage is aiding the input voltage, the feedback is positive. A comparator using positive feedback is usually called a Schmitt Trigger. Schmitt Trigger is used as a squaring circuit, in digital circuitry, amplitude comparator, etc.

Circuit diagram

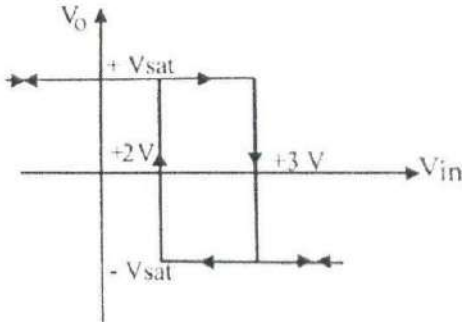
Schmitt trigger LTP = 2V and UTP =3V



Waveform



Transfer Characteristics



Design:

Schmitt trigger LTP=-2V and UTP=+3V

Let the required LTP be -3V and UTP be+3V

Assume, V_{sat}=+13V when V+=15V as reference voltage.

LTP=2V=($-13R_2/(R_1+R_2)$)+(V_{ref} $R_1/(R_1+R_2)$)

UTP=+3V=($13R_2/(R_1+R_2)$)+(V_{ref} $R_1/(R_1+R_2)$)

Assume $R_2 \cong 1K$ and $R_1 \cong 22K$, we get reference voltage V_{ref} =2.5 V

Procedure:

1. Verify whether the op-amp was in good condition.
2. Set up the circuit for Schmitt trigger and switch on the supplies and observe the input and output on the CRO screen.
3. Observe the transfer characteristics.

Result : Designed the Schmitt trigger and obtained the output

Exp No: 04
Date:

Astable and Monostable multivibrator using Op –Amps

Aim: To design set up a astable and monostable multivibrators using op-amps for a frequency of 1kHz.

Components required: Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

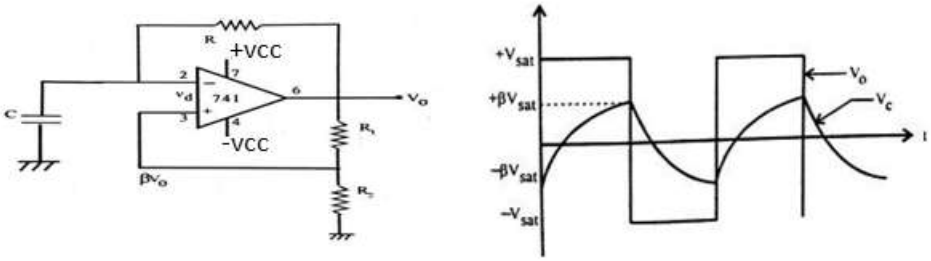
Theory:

Astable multivibrator: Astable multivibrators are capable of producing square wave for given frequency, amplitude and duty cycle. The output of an op-amp is forced to swing repetitively between positive saturation +Vsat and negative saturation –Vsat resulting in asquare wave output. This circuit is also called free running multivibrator or square wave generator. The output of the op-amp will be in positive saturation if differential input voltage is negative and vice versa. The differential voltage Vd = Vc -βVsat where β is the feedback factor. βVsat is the potential at non-inverting terminal of op-amp. Consider the instant at which Vo=+Vsat. Now the capacitor charges exponentially towards +Vsat through R. Automatically Vd increases and crosses zero. This happens when Vc changes to –Vsat. Now capacitor starts to discharge to zero and recharge towards –Vsat. Now Vd decreases and crosses zero. This happens when Vc=-βVsat. The moment Vd becomes negative again, output changes to +Vsat. This completes one cycle. The time period T of the square wave is $T= 2RC\ln(1+\beta)/(1-\beta)$.If β is made ½, T= 2.2RC. Astable multivibrator is particularly useful for the generation of frequency in the audio frequency range. Higher frequencies are limited by the delay time and slew rate of the op-amp.

Monostable multivibrator: A Monostable Multivibrator, often called a one-shot Multivibrator. It ha a stable state and and a quasi stable state. The circuit remains in stable state until triggering signal causes a transition to quasi stable state. After a time interval, it returns to the stable state. So a single pulse of predetermined duration can be generated using this circuit. Consider the instant at which the output Vo=+Vsat. Now the diode D1 clamps the capacitor voltage Vc at 0.7V. feedback voltage available at non inverting terminal is +βVsat. When the negative going trigger is applied such that potential at non inverting terminal becomes less than
0.7 V , the output switches to –Vsat. Now the capacitor charges through R towards –Vsat, because the diode becomes reverse biased. When the capacitor voltage become more negative than –Vsat, the comparator switches back to +Vsat, and the capacitor C starts charging to +Vsat through R until Vc reaches 0.7.

Circuit diagrams and waveforms :

Astable multivibrator



DESIGN

Required period of oscillation T=1ms with duty

cycle 50% Time period T =T_1+T_2 = 2RC

ln(1+β)/(1-β)

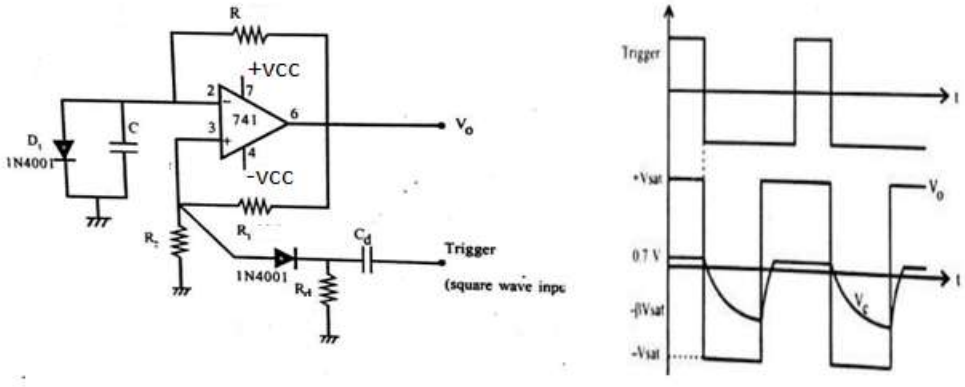
Where β, the feedback factor=R_2/(R_1+R_2)

Assume β=0.5 and R_2≅10K. Then R_1≅10K.

When β=0.5, T=2.2RC

Assume C be 0.1μF. Then R≅ 4.7K.

Monstable multivibrator



DESIGN

Required period of oscillation T=1ms with duty

cycle 50% Time period $T = RC \ln[1/(1-\beta)]$

$T=0.69RC$

Where β, the feedback factor=$R_2/(R_1+R_2)$

Assume, β=0.5 and $R_2 \cong 10K$. Then $R_1 \cong 10K$.

Let C be 0.1μF. Then $R \cong 14.5K$. Use 15 K

Design of differentiating circuit: $R_dC_d<0.016T_t$.

Take trigger time period T_t=5ms and C_d=0.01μF Then R_d=8.2K

Procedure:
1. Verify the conditions of op-amp.

2. Set up the circuit astable multivibrator and observe the output waveform. Note down their frequencies and amplitudes.

3. Set up the circuit monostable multivibrator and feed 6Vpp,200Hz square wave at the trigger input and observe the output waveform. Note down their frequencies and amplitudes.

Results: Designed the astable and monostable multivibrator using opamp.

Exp No: 05
Date:

Timer IC NE555

Aim: To study NE555 Timer and to design and setup an astable multivibrator and monostable multivibrator using NE555 timer for a frequency of 1KHz.

Components required: NE555 timer, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory: The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation introduced this device as SE555/NE555 in 1971. The 555 timer is available with the supply voltage between +4.5 to +18v, supply current 3 to 6 mA. It is compatible with both TTL and CMOS logic circuits. The functional block diagram of 555 consist of two comparators, a flip-flop, an output stage, two BJT Q_1 and Q_2 and a voltage divider network. The comparators are devices whose outputs are HIGH when the positive(+) input voltage is greater than the negative (-) input voltage and LOW when the negative (-) input voltage is greater than positive (+) input voltage. The voltage divider consisting of three 5KΩ resistors provide a trigger level of $1/3V_{CC}$ and a threshold levels of $2/3V_{CC}$. The control voltage input can be used externally adjust the trigger and threshold levels to other values, if necessary.

When the normally HIGH trigger input momentarily goes below $1/3V_{CC}$, the output of comparator 2 switches from LOW to HIGH and set the S-R flip flop, causing the output to go HIGH and turning the discharge transistors Q_1 OFF. The output will remain HIGH until the normally LOW threshold input goes above $2/3V_{CC}$ and causes the output of comparator 1 to switch from LOW to HIGH. This resets the flip flop, causing the output to go back LOW and turning the discharge transistor ON. The external reset input can be used to reset the flip flop independent of threshold circuit. The trigger and threshold inputs are controlled by external components connected to produce either monostable or astable action.

So the output of timer becomes HIGH when the trigger input voltage is less than $1/3V_{CC}$ and the output becomes LOW when the threshold voltage is greater than $2/3V_{CC}$. Also in stable state, the output of timer is LOW.

Astable multivibrator: When the power supply V_{CC} is connected, the external timing capacitor ‘C” charges towards V_{CC} with a time constant (R_A+R_B) C. During this time, pin

Exp No: 05
Date:

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When the normally HIGH trigger input momentarily goes below $1/3V_{CC}$, the output of comparator 2 switches from LOW to HIGH and set the S-R flip flop, causing the output to go HIGH and turning the discharge transistors Q_1 OFF. The output will remain HIGH until the normally LOW threshold input goes above $2/3V_{CC}$ and causes the output of comparator 1 to switch from LOW to HIGH. This resets the flip flop, causing the output to go back LOW and turning the discharge transistor ON. The external reset input can be used to reset the flip flop independent of the threshold circuit. The trigger and threshold inputs are controlled by external components connected to produce either monostable or astable action.

So the output of timer becomes HIGH when the trigger input voltage is less than $1/3V_{CC}$ and the output becomes LOW when the threshold voltage is greater than $2/3V_{CC}$. Also in a stable state, the output of timer is LOW.

Astable multivibrator: When the power supply V_{CC} is connected, the external timing capacitor 'C" charges towards V_{CC} with a time constant (R_A+R_B) C. During this time, pin 3 is high ($\approx V_{CC}$) as Reset R=0, Set S=1 and this combination makes Q =0 which has unclamped the timing capacitor 'C'.

When the capacitor voltage equals 2/3 V_{CC}, the upper comparator triggers the control flip

flop on that Q =1. It makes Q1 ON and capacitor ‘C’ starts discharging towards ground through R_B and transistor Q1 with a time constant R_BC. Current also flows into Q1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$

During the discharge of the timing capacitor C, as it reaches Vcc/3, the lower comparator is triggered and at this stage S=1, R=0 which turns Q =0. Now Q =0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 Vcc and 1/3 Vcc respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 Vcc to 2/3 Vcc.

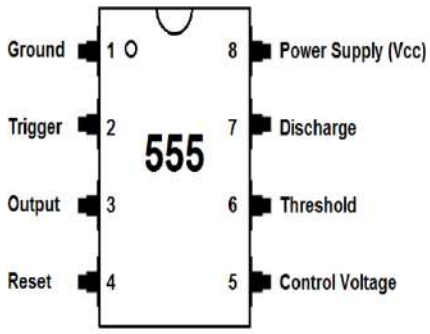
The charging period of capacitor = 0.69 (R_A + R_B) C.

The discharging period of capacitor = 0.69 R_B C.

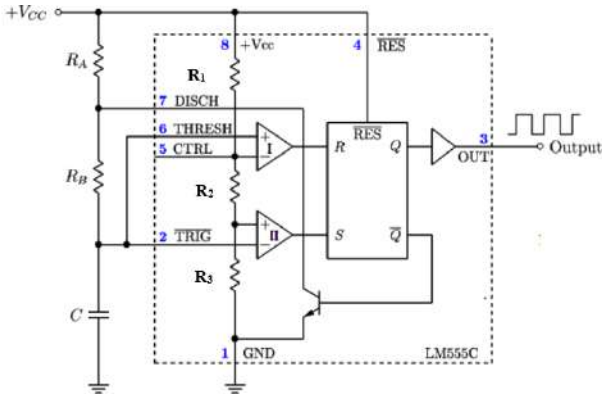
Monostable multivibrator: A monostable multivibrator, often called a one-shot multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode Q is high and in turn, Q1 is turned ON and output is low. When the negative going trigger passes through Vcc/3, the FF is set i.e. Q =0. This makes transistor Q1 off. The capacitor starts charging towards Vcc, which was earlier clamped to zero. After a time period, the capacitor voltage becomes greater than 2/3 Vcc and upper comparator resets the FF, i.e. R=1, S=0. This makes Q =1. In turn the transistor Q1 turns ON and thereby discharging the capacitor C rapidly to ground potential. Mononostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low.

Circuit diagram:

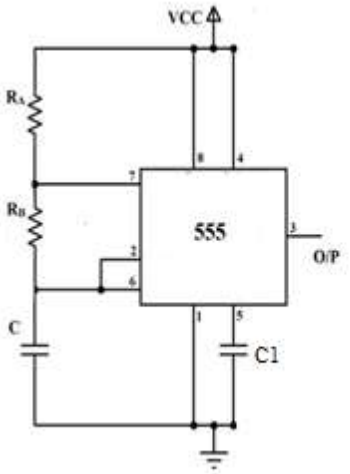
Pin out of 555 timer IC

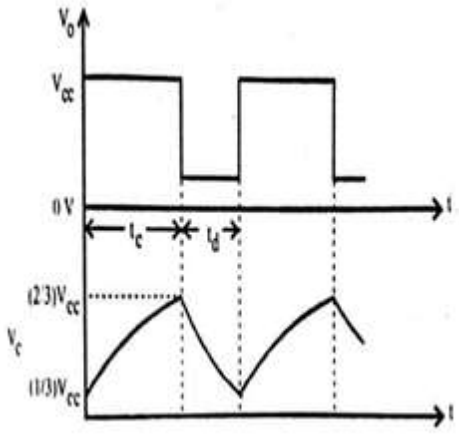


Functional block diagram of 555 timer

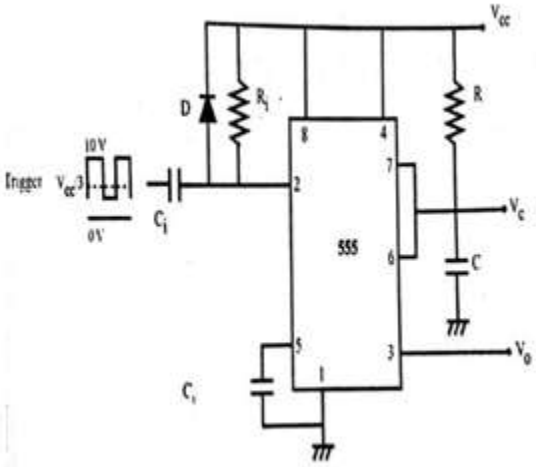


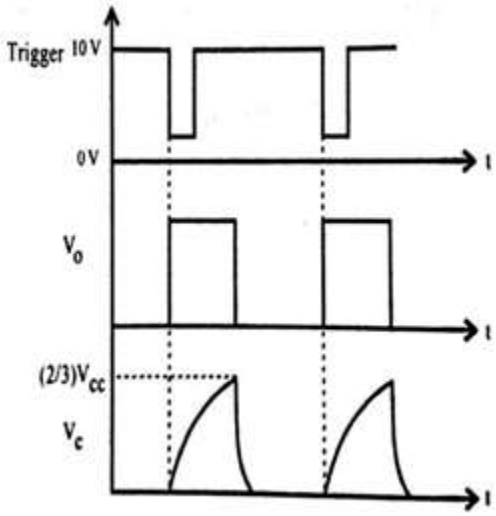
Astable multivibrator using 555 timer





Monostable multivibrator using 555 timer





Design:

1.Astable multivibrator

Take V_{CC}=10V and t_c=1ms and t_d=0.5ms

We have, t_c=0.69(R_A+R_B)C and t_d=0.69R_B

The R_A and R_B should be in the range of 1K to 10K to limit the collector current of the internal transistor.

Take appropriate values for C and C_1.

2.Monostable multivibrator

Take V_{CC}=10V and T=1ms.

We have, T=1.1RC

Take appropriate values for R and C to limit current through the internal.

Design of triggering circuit we have $R_iC_i \leq 0.0016T_t$ where T_t is the time period of the trigger.

Take appropriate values for T_t, R_i, C_i and C_1

Procedure:

1.Set up the astable multivibrator circuit after verifying the condition of the IC

2.Observe the output waveform at pin no.3 and 6 of the IC.

3. Set up the monostable multivibrator circuit.

4. Use positive pulses of amplitude Vcc and frequency 300 Hz as the trigger.

5. Observe the output waveform at pin no.3 and 6 of the IC

Result: Familiarized the NE555 Timer and designed an astable multivibrator and monostable multivibrator using NE555 timer for a frequency of 1KHz

Exp No: 06
Date:

IC voltage regulators.

Aim: To design and set up a low voltage and a high voltage regulator using IC RC723.

Components required: Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

Theory: 723 is a general purpose regulator that can be adjusted over a wide range of both positive and negative regulated voltage. It has two sectios 1- a zener diode, a constant current source and a reference amplifier that produces a fixed voltage of 7.15 at the terminal $V_{ref.}$. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage. 2- it consist of an error amplifier, a series pass transistor Q_1 and a current limiting transistor Q_2 .The error amplifier compares a sample of the output voltage applied at the INV input terminal. The error signal controls the conduction of Q_1. These two sections are not internally connected but various points are brought out on the IC package.723 regulator IC are available in a 14 pin dual in line package or 10 pin metal can. It is inherently a low current device, but it can be boosted to provide 5A or more current by connecting external components. But it has no built in thermal protection .It also has no short circuit current limits. It can operate with an input voltage from 9.5V to 40V and provide output voltage from 2V to 37V.

Low voltage regulator: A positive low voltage regulator using 723 is as shown. The voltage at NI terminal of the error amplifier due to R_1R_2 divider is $V_{IN}= V_{ref}(R_2/R_1+R)$. The difference between V_{IN} and the output voltage V_0 is directly fed back to the INV terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q_1 so as to minimize the difference the NI and INV input of error amplifier. Since Q_1 is operating as an emitter follower $V_0=V_{ref}(R_2/R_1+R_2)$. If the output voltage becomes low, the voltage at the INV terminal of the error amplifier also goes down. This makes the output of the error amplifier to become more positive, thereby driving transistor Q_1 more into conduction .This reduces the voltage across Q_1 and drive more current into the load causing the voltage across the load to increase. So the initial drop in the load voltage has been compensated. Similarly any increase in load voltage, or changes in the input voltage get regulated. The reference voltage typically 7.15volt, so the output voltage $V_0=7.15(R_2/R_1+R_2)$. This will be always being less than 7.15V.

High voltage regulator:

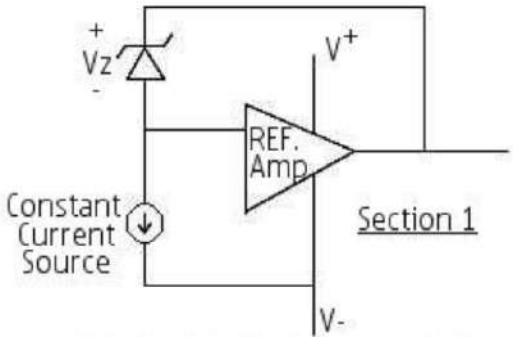
If it is desired to produce regulated output voltage greater than 7V, a small change should be made in the circuit for low voltage regulator. The non-inverting terminal is

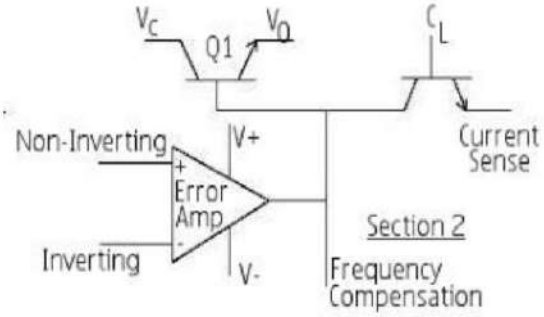
connected directly to V_{ref} through R3. So the voltage at the non-inverting terminal is V_{ref}. The error amplifier operates as a non-inverting amplifier with a voltage gain of $Av=1+R_1/R_2$. Notice that Av is always greater than 1. So the output voltage of the circuit is

$$Vo=7.15(1+R_1/R_2)$$

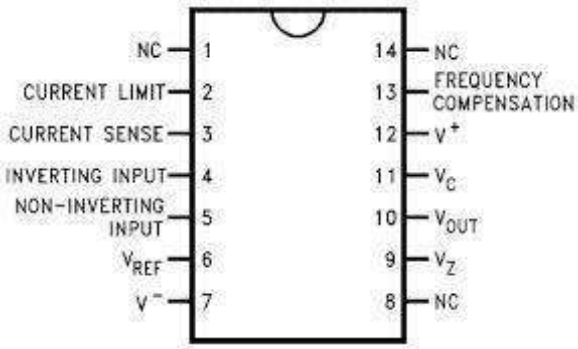
Circuit diagram

Functional block diagram of 723 regulator

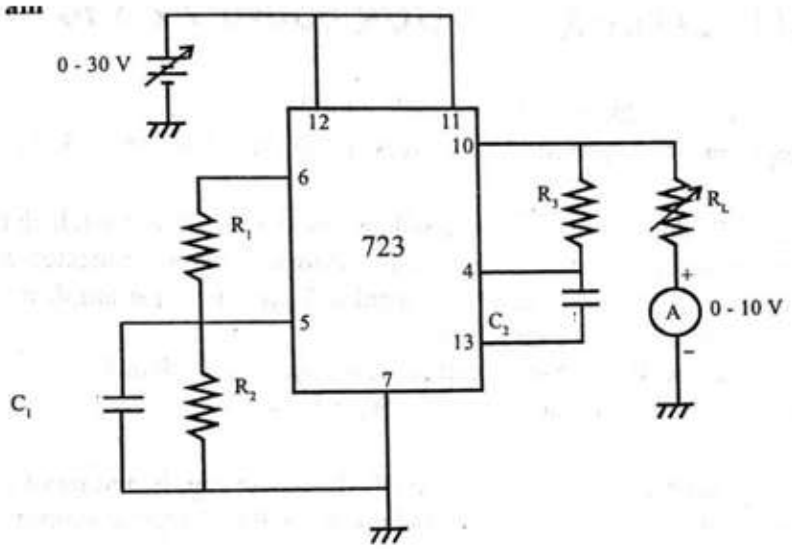




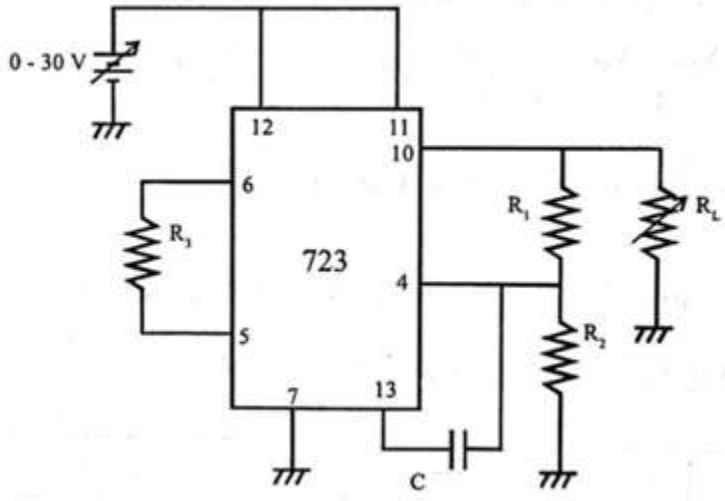
Pin diagram of IC 723



Low voltage regulator



High voltage regulator



Design

Low voltage regulator

$V_0 = 7.15$
$R2/(R1+R2) = 6V$

$R1=(Vref – V_0)/I_D$
$R2=V_0/I_D$
Take appropriate values for C and R3

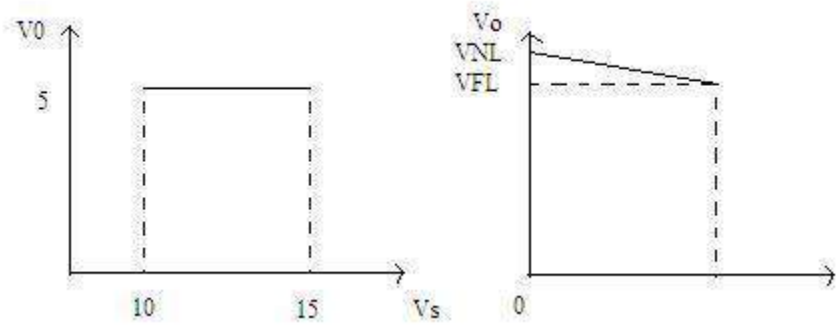
High voltage Regulator

$V_0 = 7.15(1 +(R1/ R2))$
Assume appropriate value for R1

Observations:

For line regulation	
V_S(V)	V_o(V)
For load regulation	
I_L(mA)	V_o(V)

Typical graph



Line regulation Load Regulation

Procedure:

Low voltage regulator:

1. Set up the circuit. Switch on the power supply and input voltage sources.
2. Vary the input voltage from 6V to 15V and observe the output voltage. Note down it in tabular column.
3. Vary the rheostat and note the change in output current.
4. Draw the regulation characteristics with input on X-axis and output on Y-axis.
5. Calculate the % line regulation using the expression: S_V = change in output voltage / change in input voltage
6. Calculate the % load regulation using the expression: $S_L = (V_{NL} – V_F)/ V_{NL}$

High voltage regulator:

1. Set up the circuit. Switch on the power supply and input voltage sources.
2. Vary the input voltage from 6V to 30V and observe the output voltage. Note down it in tabular column.
3. Vary the rheostat and note the change in output current.
4. Draw the regulation characteristics with input on X-axis and output on Y-axis.

Result:

Designed the voltage regulator circuits using IC

723 Load regulation for

Low voltage regulator =……

High voltage regulator=……

Exp No: 07
Date:

A/D converters- counter ramp and flash type.

Aim: To design and setup a counter ramp and flash type ADC.

Components required: Op-amp, diode, resistors, capacitors, comparator LM311,IC's 7408,7493,741, breadboard, CRO, function generator and power supplies.

Theory:

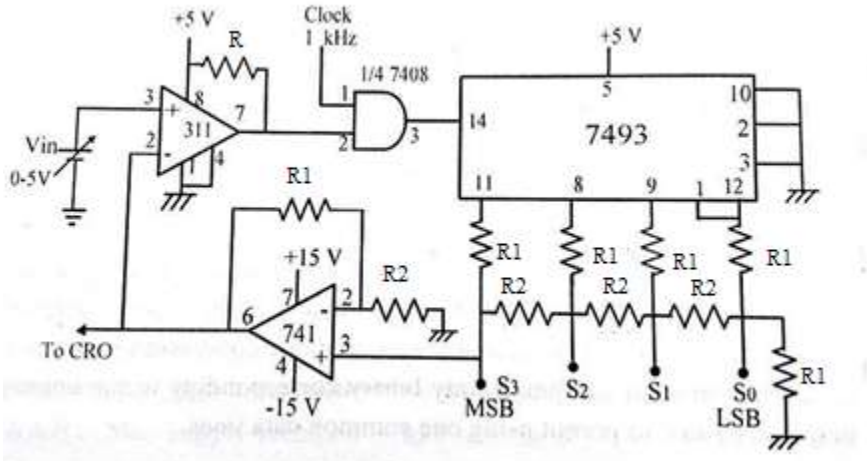
Counter ramp ADC: It displays the digital equivalent of input analog signal. Basically, a comparator opens a gate for a period of time and a counter counts the number of pulses flowing through the gate. Comparator keeps the gate open until the analog equivalent of the digital output of the counter equals the input voltage that to be digitized.

A four bit binary counter 7493 is used to count the pulses. An op amp with R-2R ladder network is used as a digital to analog converter. Comparator output provides high output as long as $V_{in} > V_a$. V_{in} is the input to be digitized and V_a. analog equivalent of the instantaneous digital output. When $V_{in} < V_a$, gate closes and pulses stop to flow to binary counter. Digital output remains standstill at its value.

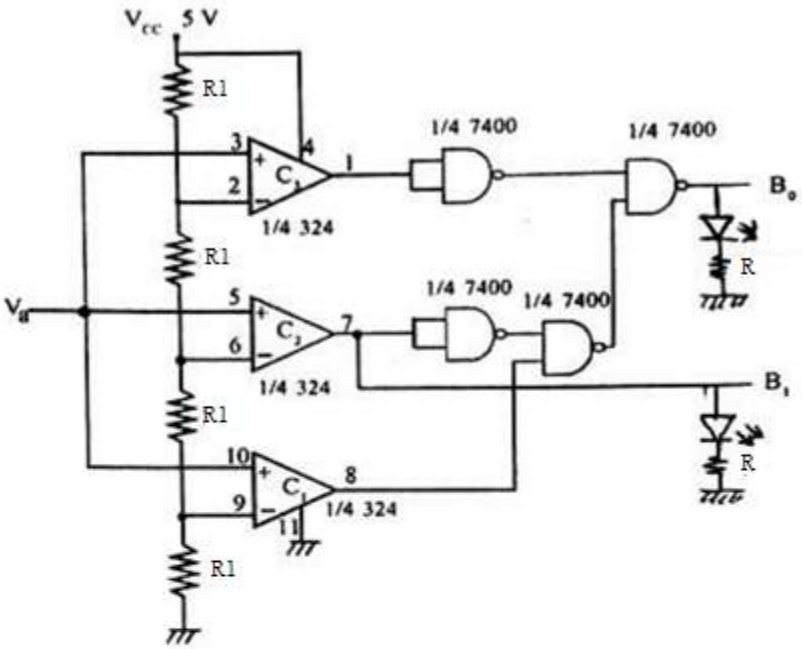
2-bit flash ADC: If the analog signal exceeds the reference signal to any comparator, that comparator turns on. If all comparators are off, analog input will be between 0 and +V/4.If C1 is high and C2 and C3 are low, input will be between +V/4 and +V/2.If C1 andC2 are high and C3 is low input will be between +V/2 and +3V/4. If all comparators are high , analog input will be between +3V/4 and +V. the outputs of three comparators are then fed to a coding network to provide 2 bits which are equivalent to the input analog voltage.

Circuit diagram:

Counter ramp ADC



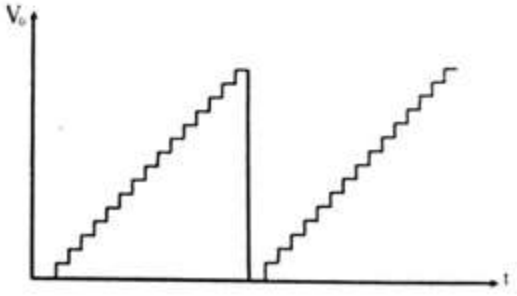
2 bit FLASH ADC



Tabular column

V (Volts)	S_3	S_2	S_1	S_0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

Waveform



Procedure:

1. Set up the circuit for counter ramp ADC and 2 bit flash ADC
2. Vary the analog input from 0 to 5V and observe the output bits.

Result:

Designed and setup the ADC circuits

Exp No: 08
Date:

D/A Converters- ladder circuit.

Aim:

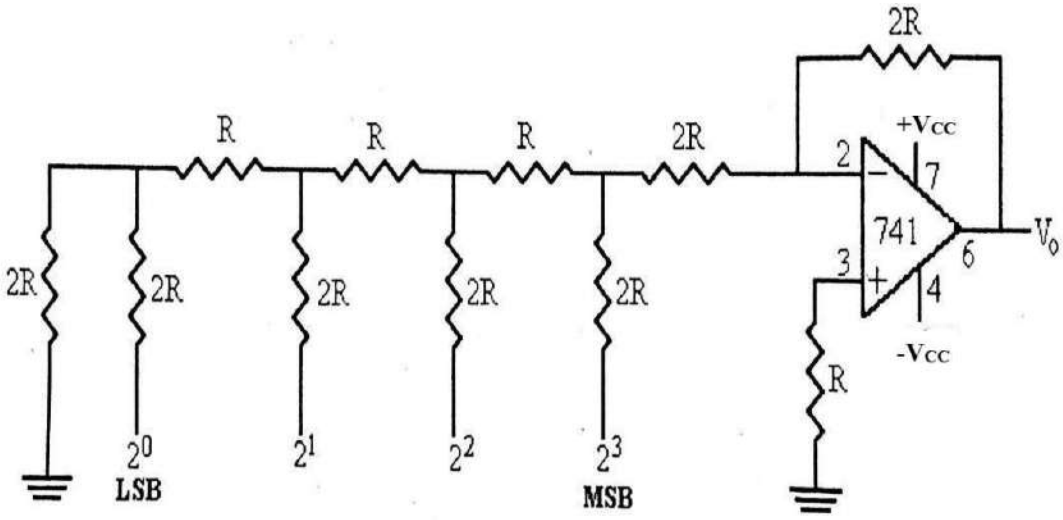
To design and set up a R-2R ladder type DAC.

Components required:

Op-amp, resistors, capacitors, breadboard, CRO, function generator and power supplies.

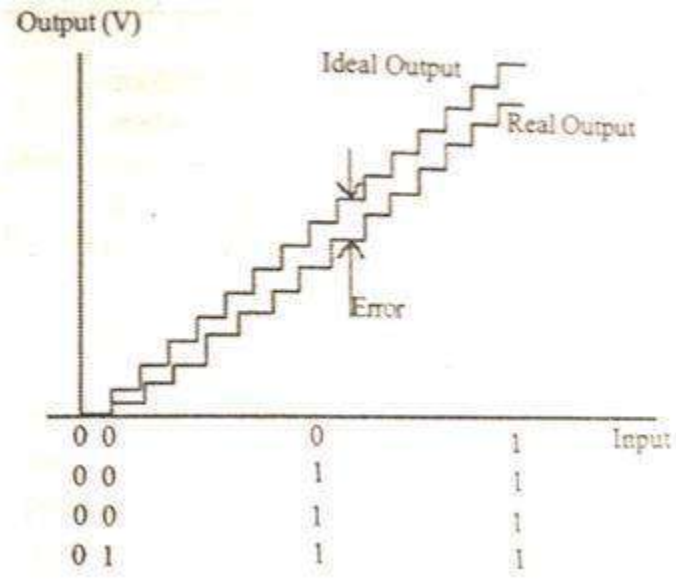
Theory: An R-2R ladder DAC uses fewer unique resistor values. Only two resistance values are used anywhere in the entire circuit. This means that only two values of resistance in the ratio 2:1.Current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same, so the incoming current splits equally along both paths. The half current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along the ladder can affect the output.

Circuit diagram:



Observations and typical response curve

	V0(Volts)



$Q_3Q_2Q_1Q_0$

0000
0001
0010
……
……
1101
1110
1111

Procedure:

1. Verify the conditions of op-amp.
2. Set up the DAC circuit and manually enter binary inputs 0000 to 1111.
3. Measure the output voltage using a multimeter and tabulate the readings.
4. Draw the response with analog output on Y-axis and binary output on X-axis.

Results:

Designed the ladder circuit DAC Error in the output: ..... %

AEL 331: PART B: Instrumentation Lab

Exp No: 01
Date:

Determination of the characteristics of RTD.

AIM:

To determine the characteristic of RTD.

APPARATUS:

1. RTD
2. Resistors
3. Op-amp IC 741
4. Thermometer
5. Electrical kettle
6. 5V power supply

THEORY:

Resistance Temperature Detector (RTD):

Resistance thermometers, also called resistance temperature detectors (RTDs), are sensors used to measure temperature. Many RTD elements consist of a length of fine wire wrapped around a ceramic or glass core but other constructions are also used. The RTD wire is a pure material, typically platinum, nickel, or copper. The material has an accurate resistance/temperature relationship which is used to provide an indication of temperature. As RTD elements are fragile, they are often housed in protective probes.
RTDs, which have higher accuracy and repeatability, are slowly replacing thermocouples in industrial applications below 600 °C.
The variation of resistance of metals with temperature is normally modeled in the form:

$$R_t = R_0\left[1 + \alpha\left(t - t_0\right) + \beta(t - t_0)^2\right]$$

where R_t and R_0 are the resistance values at t°C and t_0 ℃ espectively;
α, β are constants that depends on the metal.
For a small range of temperature, the expression can be approximated as:

$$R_t = R_0\left[1 + \alpha\left(t - t_0\right)\right]$$

For Copper, $\alpha = 0.00427/℃$.
Copper, Nickel and Platinum are mostly used as RTD materials. The range of temperature measurement is decided by the region, where the resistance-temperature

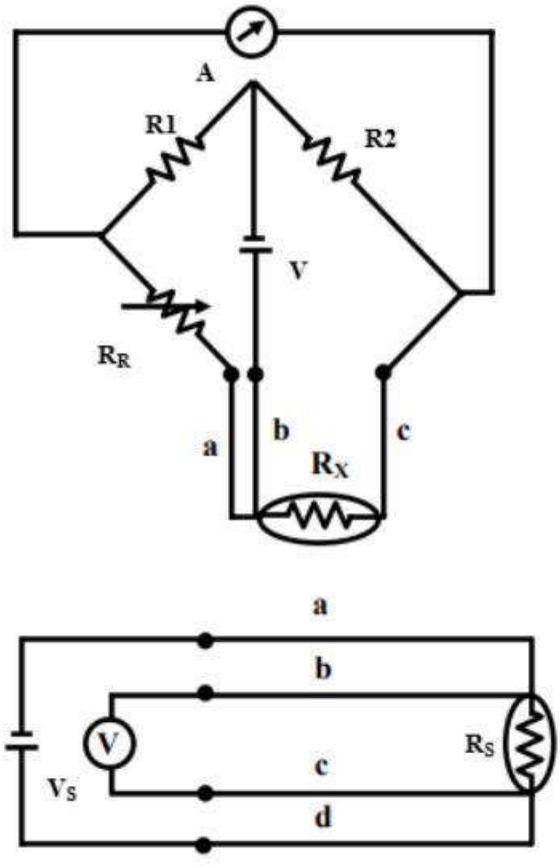
• The resistance wire is often put in a stainless steel well for protection against mechanical hazards. This is also useful from the point of view of maintenance, since a defective sensor can be replaced by a good one while the plant is in operation.

• Heat conducting but electrical insulating materials like mica is placed in between the well and the resistance material.

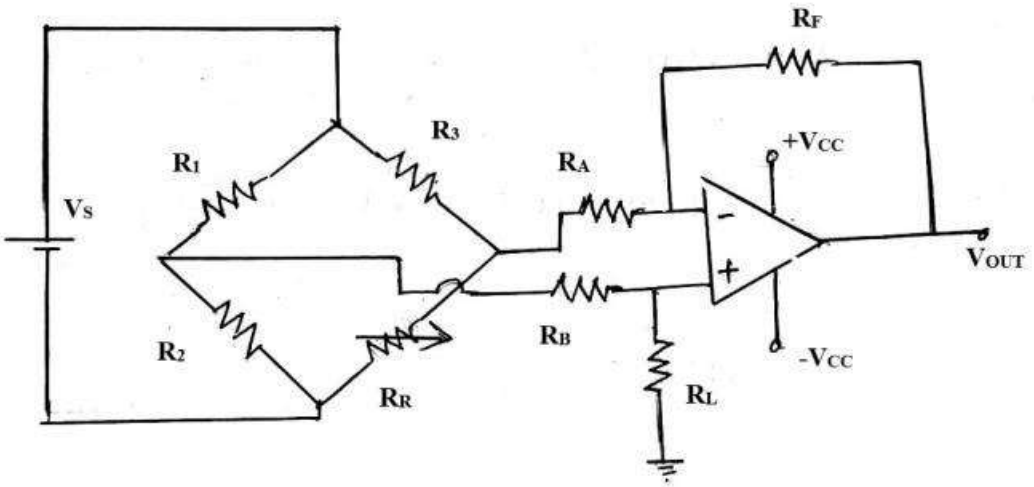
• The resistance wire should be carefully wound over mica sheet so that no strain is developed due to length expansion of the wire.

Signal conditioning :

The resistance variation of the RTD can be measured by a bridge, or directly by volt-ampere method. But the major constraint is the contribution of the lead wires in the overall resistance measured. Since the length of the lead wire may vary, this may give a false reading in the temperature to be measured. There must be some method for compensation so that the effect of lead wires is resistance measured is eliminated. This can be achieved by using either a three wire RTD, or a four wire RTD. Both the schemes of measurement are shown in figure. In three wire method one additional dummy wire taken from the resistance element and connected in a bridge so that the two lead wires are connected to two adjacent arms of the bridge, thus canceling each other's effect. The four wire method of measurement is shown in figure below. It is similar to a four terminal resistance and two terminals are used for injecting current, while two others are for measuring voltage.



CIRCUIT DIAGRAM:



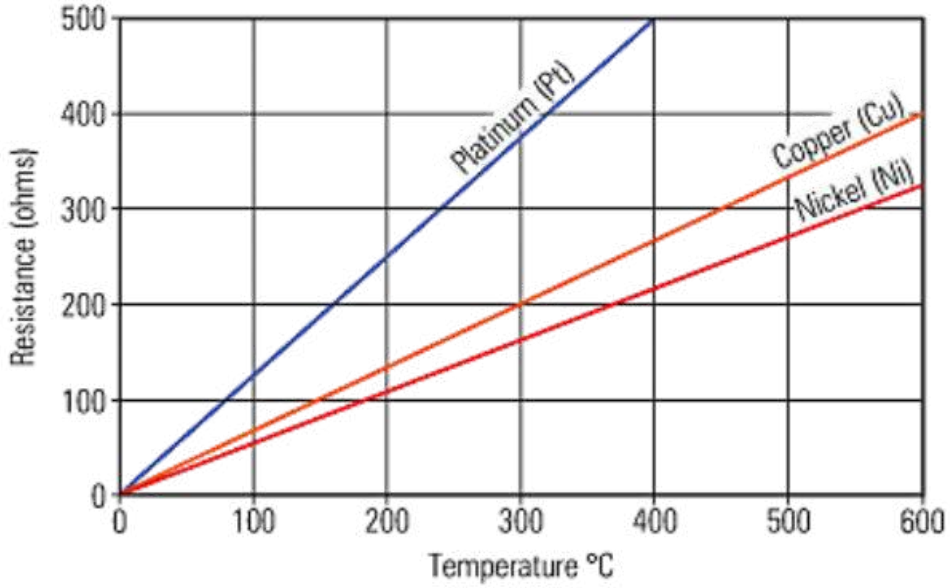
PROCEDURE:

1. Connect the circuit diagram as shown in figure. (Check the opamp using buffer circuit before using the circuit.)
2. Connect the kettle full with $^{3}/_{4}$ of the kettle and immerse the thermometer and RTD to it.
3. Note down the water temperature using the thermometer.
4. Note down the corresponding output voltage in the multimeter.
5. Similarly note down reading from multimeter for different temperature up to 100 °C.
6. Graph is plotted using the values obtained.
7. Observe the graph.

OBSEVATION:

Temperature (°C)	Output voltage (mV)
30	
35	
40	
45	
50	
60	
70	
80	
90	
100	

Model Graph:



RESULT:
Determined the characteristics of optical transducer using RTD.

Exp No: 02
Date:

Determination of the characteristics of Thermocouple.

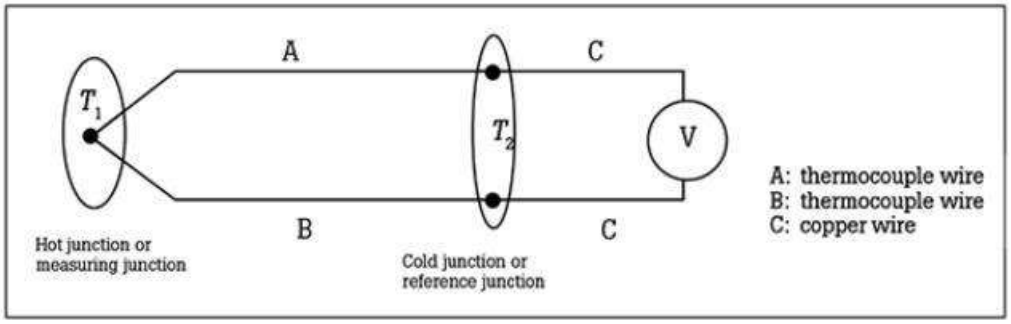
AIM:
To determine the characteristics of thermocouple.

APPARATUS:

1. Thermocouple
2. Resistors
3. Op-amp IC 741
4. Thermometer
5. Power Chord.
6. Digital multi meter

THEORY:
Theory Of Thermocouple :

The thermocouple is one of the simplest and most commonly used methods of measuring process temperatures. The operation of a thermocouple is based upon Seeback effect which states that when heat is applied to junction (hot junction) of two dissimilar metals, an emf is generated which can be measured at the other junction (cold junction). The two dissimilar metals form an electric circuit, and a current flows as a result of the generated emf as shown in Figure below.



The emf produced is function of the difference in temperature of hot and cold junctions and is given by: **$E = a\Delta\theta$**

Where a = photoelectric constant.

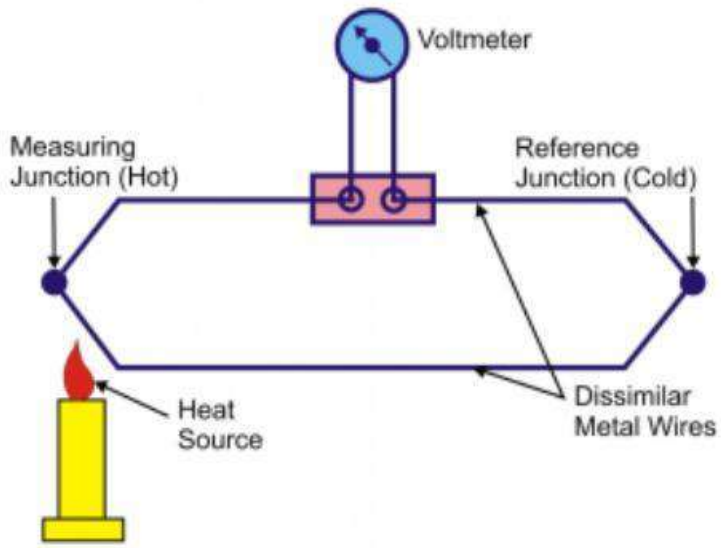
$\Delta\theta$ = difference between temperatures of hot and cold junctions.

J-type thermocouple :

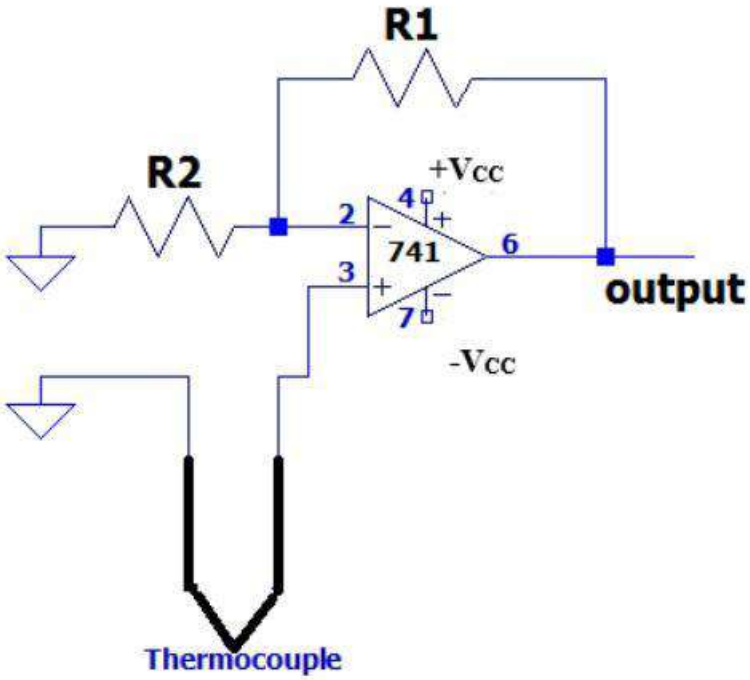
This active transducer is made of Iron and Constantan metals. There are two junctions, one kept as a reference and the other is subjected to the temperature. Depending on the difference in the temperature of the two junctions, it develops an output voltage without the need of any excitation. Hence is called an active transducer on the principle of seeback effect. The output voltage is in millivolts. This voltage is suitably signal conditioned to give an output in volts. The thermocouple senses the temperature from the temperature source (Water bath) in terms of millivolts. This millivolts output which is obtained from thermocouple is given to inverting amplifier for further amplification. This amplifier amplifies the given millivolts in the range of (0- 3.5) V.

Thomson effect :

The evolution or absorption of heat when electric current passes through a circuit composed of a single material that has a temperature difference along its length. This transfer of heat is superimposed on the common production of heat associated with the electrical resistance to currents in conductors.



CIRCUIT DIAGRAM:



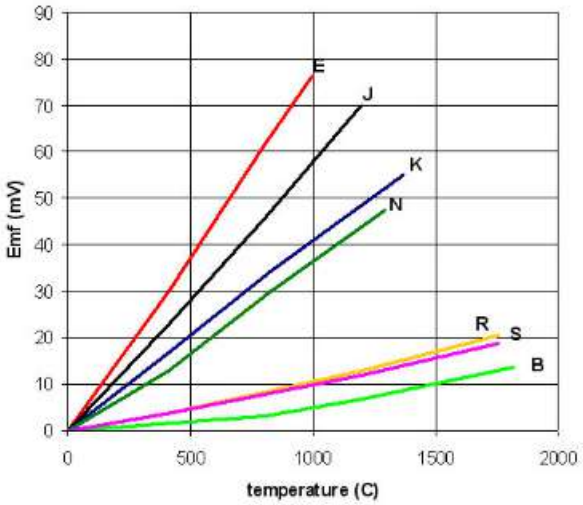
PROCEDURE:

1. Set up the circuit as per the diagram.
2. Check the op-amp by arranging buffer circuit (Gain = 1).
3. Connect the kettle full with $^{3}/_{4}$ of the kettle and immerse the thermometer and thermocouple to it.
4. Note output voltage from multimeter for different temperature (up to $100^{\circ}C$).
5. Draw the graph with temperature at x axis and output voltage as y axis.

OBSEVATION:

Temperature (℃)	Output voltage (mV)
30	
40	
50	
60	
70	
80	
90	
100	

Model graph:



RESULT:
Determined the characteristics of Thermocouple.

Exp no: 03
Date:

Measurement of Strain and Load using Strain Gauge.

AIM:

To measure strain and load using Strain gauge.

APPARATUS:

strain measuring Strain kit, Load measurement associated weight.

THEORY:

A Strain gauge is a sensor whose resistance varies with applied force; it converts force, pressure, tension, weight, etc., into a change in electrical resistance which can then be measured. When external forces are applied to a stationary object, stress andstrain are the result. The gauge is attached to the object by a suitable adhesive, such as cyanoacrylate. As the object is deformed, the foil is deformed, causing its electrical resistance to change. This resistance change, usually measured using a Wheatstone bridge, is related to the strain by the quantity known as the *gauge factor*.

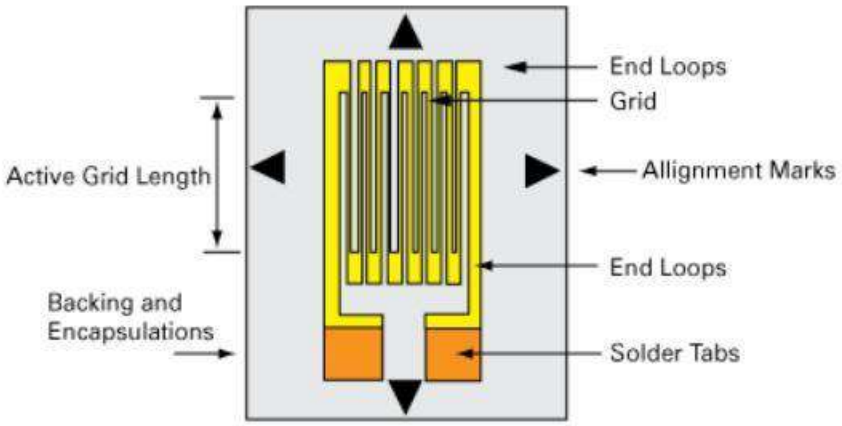
strain gauge takes advantage of the physical property of electrical conductance and its dependence on the conductor's geometry. When an electrical conductor is stretched within the limits of its elasticity such that it does not break or permanently deform, it will become narrower and longer, which increases its electrical resistance end-to-end. Conversely, when a conductor is compressed such that it does not buckle, it will broaden and shorten, which decreases its electrical resistance end-to-end. From the measured electrical resistance of the strain gauge, the amount of induced stress may be inferred.

A typical strain gauge arranges a long, thin conductive strip in a zig-zag pattern of parallel lines. This does not increase the sensitivity, since the percentage change in resistance for a given strain for the entire zig-zag is the same as for any single trace. A single linear trace would have to be extremely thin, hence liable to overheating (which would change its resistance and cause it to expand), or would need to be operated at a much lower voltage, making it difficult to measure resistance changes accurately.

- $Strain = e = {\Delta L}/{L}$
- *Poisson's ratio =* $\gamma = \frac{e_L}{e_T}$
- $Gauge\ Factor = G = \frac{{\Delta R}/{R}}{{\Delta L}/{L}} = \frac{{\Delta R}/{R}}{e}$
- $stress = {-F}/{A}$

Where,

$$F = force, e = strain, A = area, R = resistance, L = length.$$



Load cell:

A load cell is a type of force gauge. It consists of a transducer that is used to create an electrical signal whose magnitude is directly proportional to the force being measured. The various load cell types include hydraulic, pneumatic, and strain gauge.

Strain gauge load cells are the most common in industry. These load cells are particularly stiff, have very good resonance values, and tend to have long life cycles in application. Strain gauge load cells work on the principle that the strain gauge (a planar resistor) deforms when the material of the load cells deforms appropriately. Deformation of the strain gauge changes its electrical resistance, by an amount that is proportional to the strain. The change in resistance of the strain gauge provides an electrical value change that is calibrated to the load placed on the load cell. A load cell usually consists of four strain gauges in a Wheatstone bridge configuration. Load cells of one strain gauge (quarter bridge) or two strain gauges (half bridge) are also available.

CIRCUIT DIAGRAM:

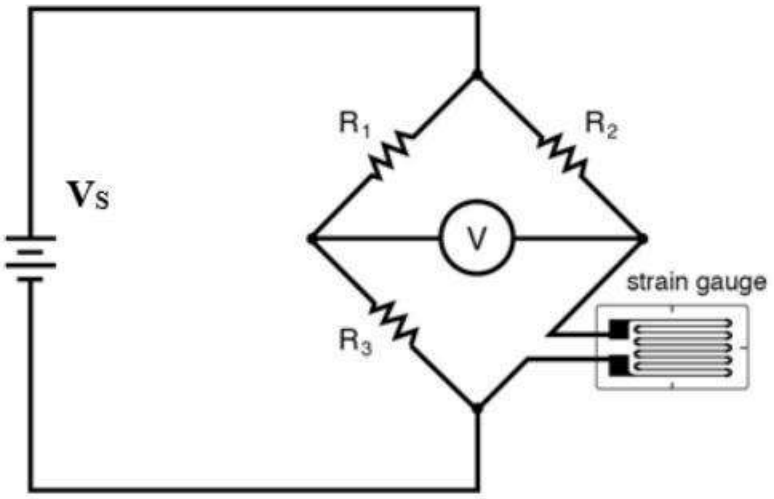


Figure 2. Quarter bridge circuit.

PROCEDURE:

1. Arrange the equipment.
2. Test the strain gauge in different load condition and do the calibration procedure.
3. Now unload it fully and calibrate.
4. Load the strain Gauge using assorted weight and received the reading.
5. After fully load, take the unloading readings.
6. Plot the graph and we may obtain straight line.

OBSEVATION:

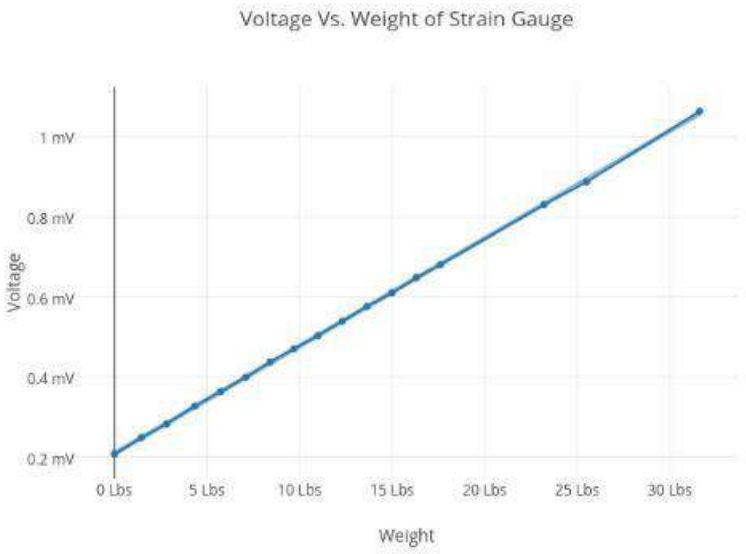
LOAD CELL:

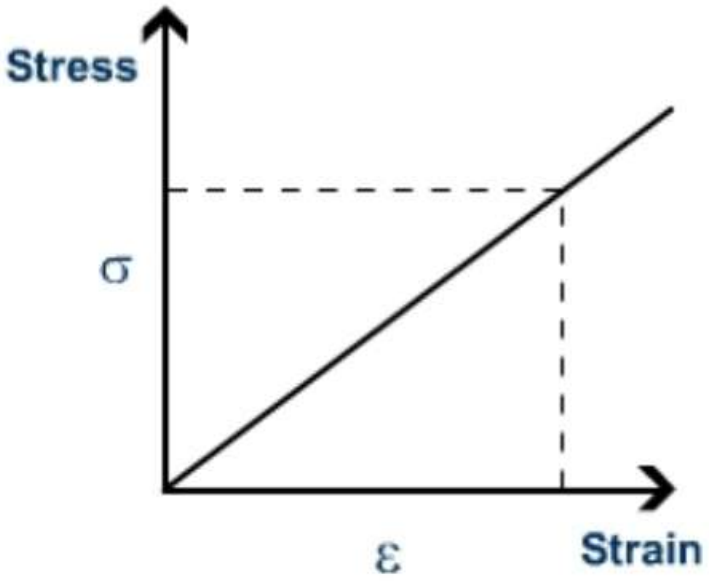
Sl.No.	Loading		Unloading		Average	
	Weight(m gm)	Voltage (mV)	Weight(m gm)	Voltage (mV)	Weight(m gm)	Voltage (mV)

Strain Measurements:

Sl.No.	Loading		Unloading		Average	
	Weight(m gm)	Strain ($\mu strain$)	Weight(m gm)	Strain ($\mu strain$)	Weight(m gm)	Strain ($\mu strain$)

Model Graph:





RESULT:
Strain and Load using strain gauge has been measured and graph has been plotted.

Exp No: 04
Date:

Determination of the characteristics of LVDT.

AIM:

To study the characteristics of LVDT

APPARATUS:

1. LVDT
2. Resistors
3. 10KΩ POT - 1
4. DMM
5. Signal generator

THEORY:

Linear variable differential transformers (LVDT) are used to measure displacement. LVDTs operate on the principle of a transformer. LVDT consists of a coil assembly and a core. The coil assembly is typically mounted to a stationary form, while the core is secured to the object whose position is being measured. The coil assembly consists of three coils of wire wound on the hollow form. A core of permeable material can slide freely through the center of the form. The inner coil is the primary, which is excited by an AC source as shown. Magnetic flux produced by the primary is coupled to the two secondary coils, inducing an AC voltage in each coil. The main advantage of the LVDT transducer over other types of displacement transducer is the high degree of robustness. Because there is no physical contact across the sensing element, there is no wear in the sensing element.

Because the device relies on the coupling of magnetic flux, an LVDT can have infinite resolution. Therefore the smallest fraction of movement can be detected by suitable signal conditioning hardware, and the resolution of the transducer is solely determined by the resolution of the data acquisition system.

The LVDT closely models an ideal zeroth-order displacement sensor structure at low frequency, where the output is a direct and linear function of the input. It is a variable-reluctance device, where a primary center coil establishes a magnetic flux that is coupled through a center core (mobile armature) to a symmetrically wound secondary coil on either side of the primary. Thus, by measurement of the voltage amplitude and phase, one can determine the extent of the core motion and the direction, that is, the displacement. Figure shows the linearity of the device within a range of core displacement. Note that the output is not linear as the core travels near the boundaries of its range. This is because less magnetic flux is coupled to the core from the primary. However, because LVDTs have excellent repeatability, nonlinearity near the boundaries of the range of the device can be predicted by a table or polynomial curve-fitting function, thus extending the range of the device.

CIRCUIT DIAGRAM:

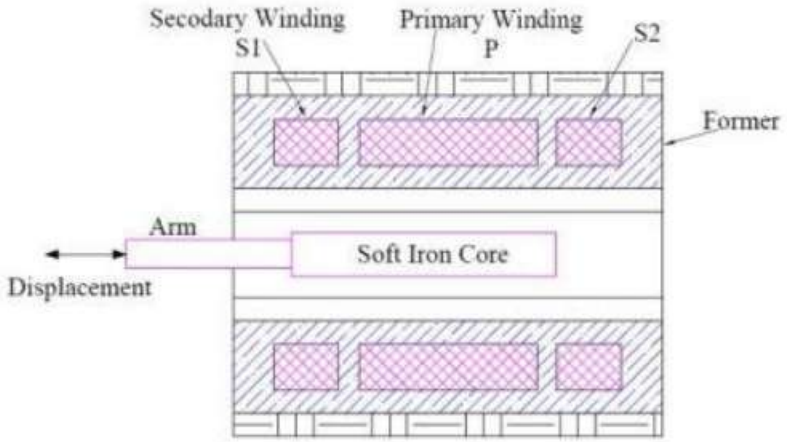
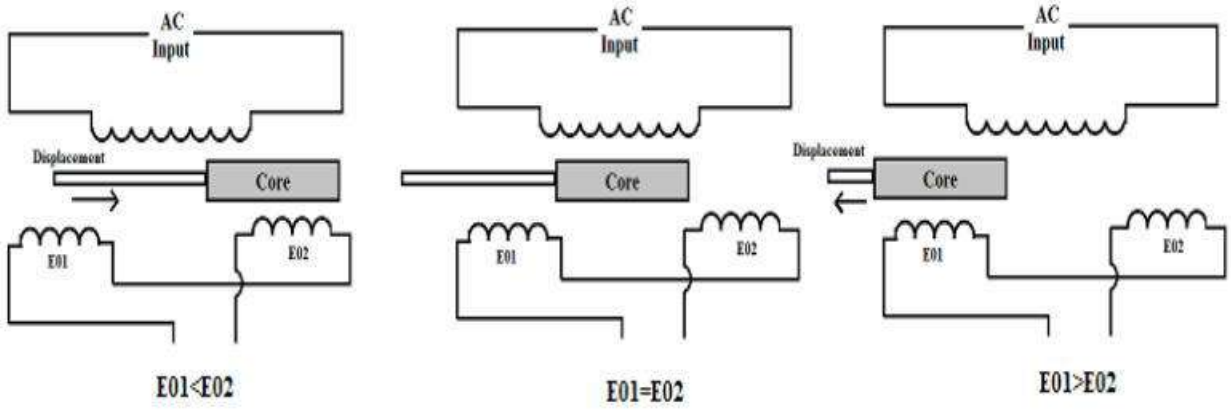


Figure 3 | Figure 2 | Figure 1



PROCEDURE:

1. Rig up the circuit as shown in figures.
2. Internally set the core of an LVDT at center position and observe the residual voltage of null position.
3. Minimize the residual voltage with external balance circuit.
4. Change the core displacement 1mm in one direction and observe the output voltage in digital multimeter.
5. Repeat the step 4 until the displacement is 5 mm, and observe the corresponding output voltage for various displacements in steps of 1mm etc.
6. Now it is moved towards other direction and repeat step 5.
7. Draw the graph for displacement Vs output voltage.

CASE I

When the core is at null position (for no displacement)

When the core is at null position then the flux linking with both the secondary windings is equal so the induced emf is equal in both the windings. So for no displacement the value of output e_{out} is zero as e_{01} and e_{02} both are equal. So it shows that no displacement took place.

CASE II

When the core is moved to upward of null position (For displacement to the upward of reference point)

In the this case the flux linking with secondary winding S_1 is more as compared to flux linking with S_2. Due to this e_{01} will be more as that of e_{02}. Due to this output voltage e_{out} is positive.

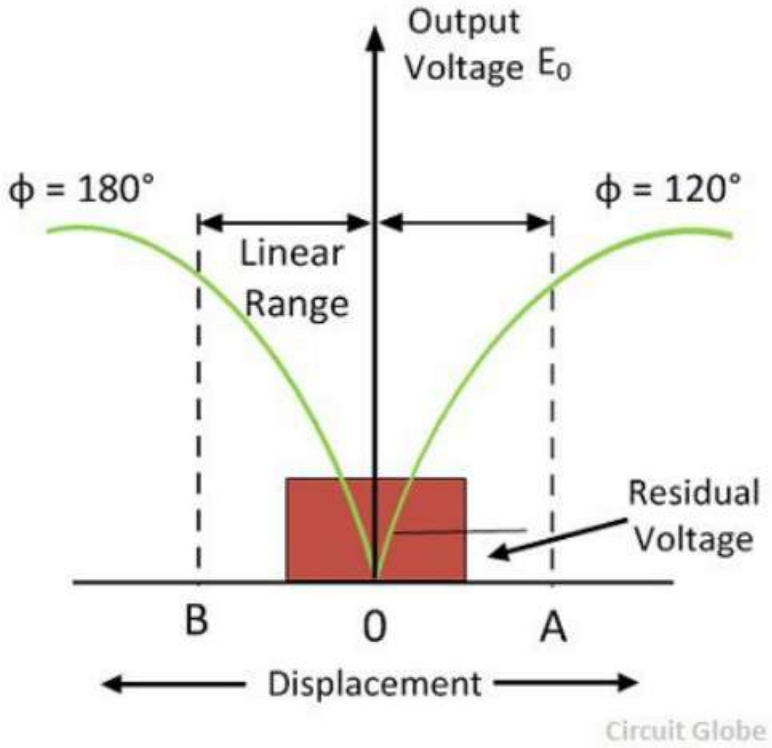
CASE III

When the core is moved to downward of Null position(for displacement to the downward of the reference point). In this case magnitude of e_{02} will be more as that of e_{01} . Due to this output e_{out} will be negative and shows the output to downward of the reference point.

OBSEVATION:

Distance (mm)	Output voltage (mV)
-5	
-4	
-3	
-2	
-1	
0	
1	
2	
3	
4	
5	

MODEL GRAPH:



RESULT:
LVDT characteristics are observed and studied.

Exp No: 05
Date:

Level measurement using capacitive transducer.

AIM:
To measure the level using capacitive transducer.

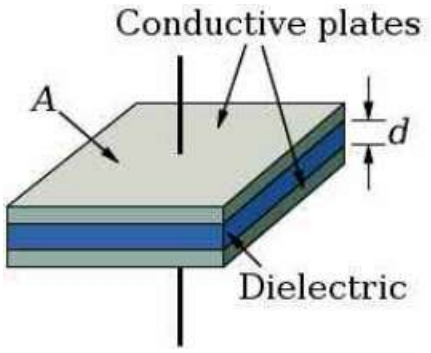
APPARATUS:
1. Capacitive Transducers
2. Resistors
3. Op-amp IC 741
4. Non conducting liquid.
5. Power supply

THEORY:

The principle of capacitive level measurement is based on change of capacitance. An insulated electrode acts as one plate of capacitor and the tank wall (or reference electrode in a non-metallic vessel) acts as the other plate. The capacitance depends on the fluid level.

The capacitive transducer contains two parallel metal plates. These plates are separated by the dielectric medium which is either air, material, gas or liquid. In the normal capacitor the distance between the plates are fixed, but in capacitive transducer the distance between them are varied.

The principle of capacitive level measurement is based on change of capacitance. An insulated electrode acts as one plate of capacitor and the tank wall (or reference electrode in a non-metallic vessel) acts as the other plate. The capacitance depends on the fluid level. An empty tank has a lower capacitance while a filled tank has a higher capacitance. A simple capacitor consists of two electrode plate separated by a small thickness of an insulator such as solid, liquid, gas, or vacuum. This insulator is also called as dielectric. Value of C depends on dielectric used, area of the plate and also distance between the plates.

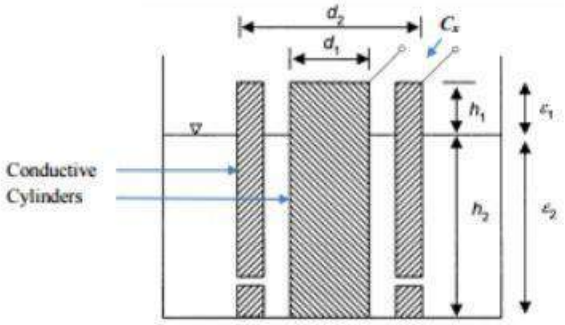


Capacitance, $C = \varepsilon \frac{A}{D}$

Where, $A = Areaoftheoverlepbetweentwoplate.$

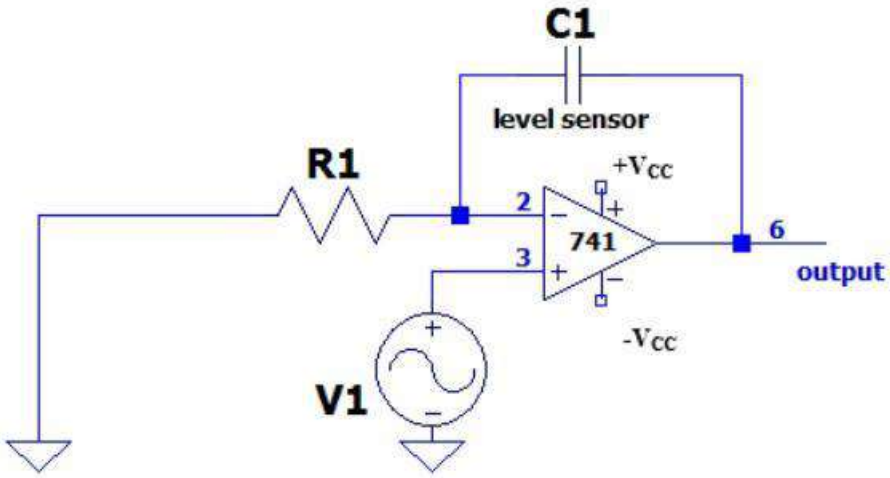
$D = Distancebetweentwoplate$.

$\varepsilon = Permittivity$.



$$C = \frac{2\pi(\varepsilon_1 \varepsilon h_1 + \varepsilon_2 \varepsilon h_2)}{ln\left(\frac{d_2}{d_1}\right)}$$

CIRCUIT DIAGRAM:



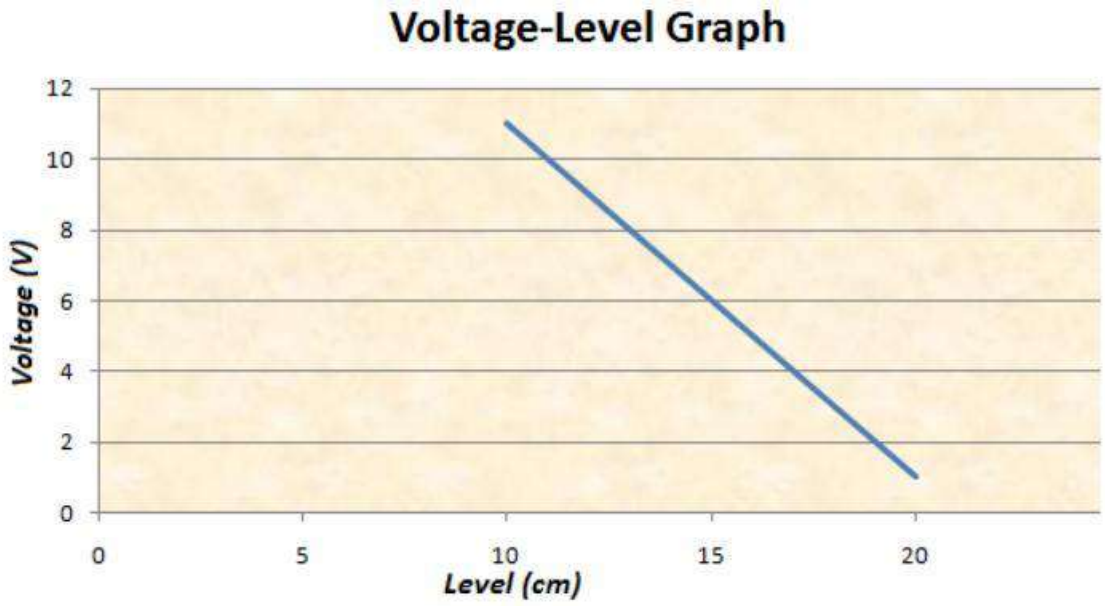
PROCEDURE:

1. Set up buffer circuit to check the gain of opamp and verify it is equal to one.
2. Set up capacitance trasducer as per circuit diagram.
3. Fill the capacitance level transducer upto about 20 cm.
4. Dram off the water at specific intervals and note down the voltage.
5. Plot the relation between the level and voltage.

OBSEVATION:

Level (cm)	Voltage (V)
20	
19	
18	
17	
15	
15	
14	
13	
12	
11	
10	

Model Graph:



RESULT:
The level is measured using capacitance transducer.

Exp No: 06
Date:

Determination of the characteristics of temperature sensor (AD590).

AIM:

To study the characteristics of Thermistor sensor (AD 590).

APPARATUS:

1. Thermistor kit AD590.
2. Heating arrangement
3. Thermometer

THEORY:

Thermistors are also called thermal resistors. For thermistor the absolute temperature- resistance relationship is given by

$$R_T = R_{T1}\, exp\left(\beta(\frac{1}{T_1} - \frac{1}{T_1})\right)$$

Where R_T = Resistance of the thermistor at absolute temperature T

R_{T1}= Resistance of the thermistor at absolute temperature T_1

β = Constant

T1 and T2 = Absolute temperatures.

Thermistors are made up of semiconductor materials. As temperature changes the resistance of materials also changes. The temperature range for thermistor is $-60°C$ to $+15\,°C$. Its resistance varies from 0.5Ω to 0.75MΩ. Thermistor is placed in contact with the media whose temperature is to be measured. As the temperature of the media changes, the resistance of the thermistor gets changed. This change of resistance can be measured by connecting the thermistor in any one arm of the Wheat stone bridge.

The AD590 is a 2-terminal integrated circuit temperature transducer that produces an output current proportional to absolute temperature. For supply voltages between 4 V and 30 V the device acts as a high-impedance, constant current regulator passing 1 µA/K. Laser trimming of the chip's thin-film resistors is used to calibrate the device to 298.2 µA output at 298.2 K (25°C).

Figure: AD590 thermistor

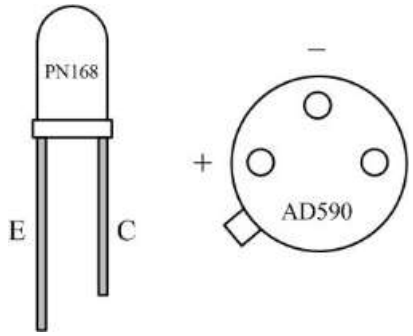
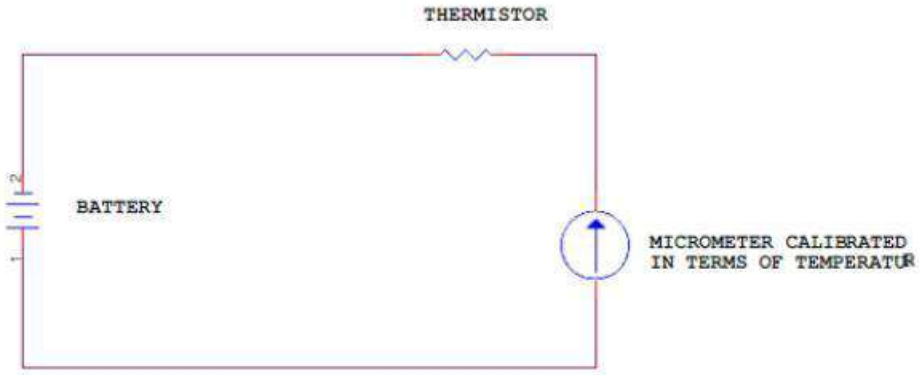


Figure: Pins/connections AD590 temperature sensor.

CIRCUIT DIAGRAM:



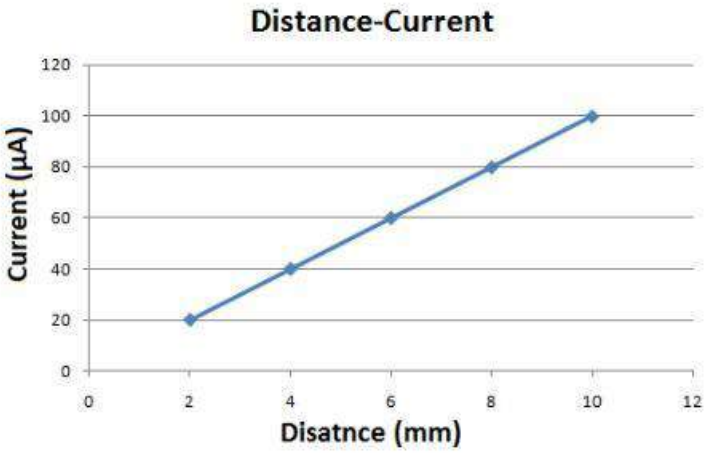
PROCEDURE:

1.Connect the main power cord at I/P main socket.
2. Switch ON the power supply .
3. Connect the thermistor sensor at the pin connector.
4. Keep the thermistor in boiling water & adjust the display ranging 100 by the adjustment span knob.

OBSEVATION:

S.No	Temperature (°C)	Display reading(mm)

Model Graph:



RESULT:

Thermistor AD590 characteristics are observed and studied.