UNIVERSITY OF KERALA

B. TECH. DEGREE COURSE

(2013 SCHEME)

SYLLABUS FOR

III SEMESTER

ELECTRONICS and COMMUNICATION ENGINEERING

SCHEME -2013

III SEMESTER

ELECTRONICS and COMMUNICATION ENGINEERING (T)

Course No	Name of subject	Credits	Weekly load, hours			C A Marks	Exam Duration Hrs	U E Max Marks	Total Marks
			L	T	D/P				
13.301	Engineering Mathematics-II (ABCEFHMNPRSTU)	4	3	1	-	50	3	100	150
13.302	Signals & Systems (AT)	4	3	1	-	50	3	100	150
13.303	Network Analysis (AT)	4	3	1	-	50	3	100	150
13.304	Analog Communications (T)	3	2	1	-	50	3	100	150
13.305	Electronic Circuits (T)	4	3	1	-	50	3	100	150
13.306	Digital Electronics (T)	4	3	1		50	3	100	150
13.307	Electronic Devices Lab (AT)	3	-	-	3	50	3	100	150
13.308	Electronic Circuits Lab (T)	3	-	-	3	50	3	100	150
	Total	**29**	**17**	**6**	**6**	**400**		**800**	**1200**

13.301 ENGINEERING MATHEMATICS - II (ABCEFHMNPRSTU)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course Objective:

This course provides students a basic understanding of vector calculus, Fourier series and Fourier transforms which are very useful in many engineering fields. Partial differential equations and its applications are also introduced as a part of this course.

Module – I

Vector differentiation and integration: Scalar and vector functions-differentiation of vector functions-velocity and acceleration - scalar and vector fields - vector differential operator-Gradient-Physical interpretation of gradient - directional derivative – divergence - curl - identities involving ∇ (no proof) - irrotational and solenoidal fields - scalar potential.

Vector integration: Line, surface and volume integrals. Green's theorem in plane. Stoke's theorem and Gauss divergence theorem (no proof).

Module – II

Fourier series: Fourier series of periodic functions. Dirichlet's condition for convergence. Odd and even functions. Half range expansions.

Fourier Transforms: Fourier integral theorem (no proof) –Complex form of Fourier integrals-Fourier integral representation of a function- Fourier transforms – Fourier sine and cosine transforms, inverse Fourier transforms, properties.

Module – III

Partial differential equations: Formation of PDE. Solution by direct integration. Solution of Langrage's Linear equation. Nonlinear equations - Charpit method. Homogeneous PDE with constant coefficients.

Module – IV

Applications of Partial differential equations: Solution by separation of variables. One dimensional Wave and Heat equations (Derivation and solutions by separation of variables). Steady state condition in one dimensional heat equation. Boundary Value problems in one dimensional Wave and Heat Equations.

References:

1. Kreyszig E., *Advanced Engineering Mathematics*, 9/e, Wiley India, 2013.
2. Grewal B. S., *Higher Engineering Mathematics*, 13/e, Khanna Publications, 2012.

3. Ramana B.V., *Higher Engineering Mathematics*, Tata McGraw Hill, 2007.
4. Greenberg M. D., *Advanced Engineering Mathematics*, 2/e, Pearson, 1998.
5. Bali N. P. and M. Goyal, *Engineering Mathematics*, 7/e, Laxmi Publications, India, 2012.
6. Koneru S. R., *Engineering Mathematics*, 2/e, Universities Press (India) Pvt. Ltd., 2012.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Five Short answer questions of 4 marks each. All questions are compulsory. There should be at least one question from each module and not more than two questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Course Outcome:

At the end of the course, the students will have the basic concepts of vector analysis, Fourier series, Fourier transforms and Partial differential equations which they can use later to solve problems related to engineering fields.

13.302 SIGNALS & SYSTEMS (AT)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course objectives:

To study the theory of signals and system. To study the interaction of signals with physical system. To study the properties of Fourier transform, Laplace transform, signal transform through linear system, relation between convolution and correlation of signals, sampling theorem and techniques, and transform analysis of LTI systems.

Module – I

Classification and Representation of Continuous time and Discrete time signals. Elementary signals, Signal operations. Continuous Time and Discrete Time Systems - Classification, Properties. Representation - Differential Equation representation of Continuous Time Systems. Difference Equation Representation of Discrete Systems.

Continuous Time LTI systems and Convolution Integral, Discrete Time LTI systems and linear convolution. Stability and causality of LTI systems. Correlation between signals, orthoganality of signals.

Module – II

Laplace Transform – ROC – Inverse transform – properties – unilateral Laplace Transform.
Frequency Domain Representation of Continuous Time Signals- Continuous Time Fourier Series and its properties Convergence. Continuous Time Fourier Transform: Properties. Relation between Fourier and Laplace Transforms. Analysis of LTI systems using Laplace and Fourier Transforms. Concept of transfer function, Frequency response, Magnitude and phase response. Energy and power spectral densities. Condition for distortionless transmission.

Module – III

Sampling of continuous time signals, Sampling theorem for lowpass signals, aliasing. Sampling techniques, Ideal sampling, natural sampling and Flat-top sampling. Reconstruction, Interpolation formula. Sampling of bandpass signals.
Hilbert Transform, Continuous time Hilbert transform, properties, Pre-envelope of continuoous time signals. Discrete time Hilbert transform.

Module – IV

Z transform – ROC – Inverse transform – properties –unilateral Z transform.
Frequency Domain Representation of Discrete Time Signals- Discrete Time Fourier Series and its properties, Discrete Time Fourier Transform (DTFT) and its properties. Relation

between DTFT and Z-Transform. Analysis of Discrete Time LTI systems using Z transforms and DTFT. Transfer function, Magnitude and phase response.

References

1. Oppenheim A. V. and A. Willsky, *Signals and Systems*, 2/e, PHI, 2009.
2. Rawat T. K., *Signals and Systems*, Oxford University Press, 2010.
3. Haykin S., *Signals & Systems*, 2/e, John Wiley, 2003.
4. Ziemer R. E., *Signals & Systems - Continuous and Discrete*, 4/e, Pearson, 2013.
5. Lathi B. P., *Principles of Signal Processing & Linear systems*, Oxford University Press, 2010.
6. Hsu H. P., *Signals and Systems*, 3/e, McGraw Hill, 2013.
7. Roberts M. J., *Signals and Systems*, 3/e, Tata McGraw Hill, 2003.
8. Kumar A., *Signals and Systems*, 3/e, PHI, 2013.
9. Chaparro L. F., *Signals and system using MATLAB*, Elsevier, 2011.
10. Yang W. W. *et. al.*, *Signals and Systems with MATLAB*, Springer, 2009.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 60% and maximum 80% Problems and Analysis.*

Course outcome:

After completion of the course students will have a good knowledge in signals, system and applications.

13.303 NETWORK ANALYSIS (AT)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course Objectives :

To make the students capable of analyzing any given electrical network. To study the transient response of series and parallel A.C. Circuits. To study the concept of coupled circuits and two port networks. To make the students learn how to synthesize an electrical network from a given impedance / admittance function.

Module – I

Network Topology, Network graphs, Trees, Incidence matrix, Tie-set matrix,Cut-set matrix and Dual networks.

Solution methods: Mesh and node analysis, Star-Delta transformation.

Network theorems: Thevenin's theorem, Norton's theorem, Superposition theorem, Reciprocity theorem, Millman's theorem, Maximum Power Transfer theorem.

Signal representation - Impulse, step, pulse and ramp function, waveform synthesis.

Module – II

Laplace Transform in the Network Analysis: Initial and Final conditions, Transformed impedance and circuits, Transform of signal waveform. Transient analysis of RL, RC, and RLC networks with impulse, step and sinusoidal inputs. Analysis of networks with transformed impedances and dependent sources.

S-Domain analysis: The concept of complex frequency, Network functions for the one port and two port - Poles and Zeros of network functions, Significance of Poles and Zeros, properties of driving point and transfer functions, Time domain response from pole zero plot.

Module – III

Parameters of two-port network: impedance, admittance, transmission and hybrid parameters, Reciprocal and Symmetrical two ports. Characteristic impedance, Image Impedance and propagation constant.

Resonance: Series resonance, bandwidth, Q factor and Selectivity, Parallel resonance. Coupled circuits: single tuned and double tuned circuits, dot convention, coefficient of coupling, analysis of coupled circuits.

Module – IV

Network Synthesis: Introduction, Elements of Realisability Theory: Causality and Stability, Hurwitz Polynomial, Positive Real Functions. Properties and Synthesis of R-L networks by the Foster and Cauer methods, Properties and Synthesis of R-C networks by the Foster and Cauer methods.

References:

1. Valkenburg V., *Network Analysis*, 3/e, PHI, 2011.
2. Sudhakar A. and S. P. Shyammohan, *Circuits and Networks- Analysis* and Synthesis, 3/e, TMH, 2006.
3. Choudhary R., *Networks and Systems,* 2/e, New Age International, 2013.
4. Kuo F. F., *Network Analysis and Synthesis,* 2/e, Wiley India, 2012.
5. Gupta B. R. and V. Singhal, *Fundamentals of Electrical Networks*, S. Chand, 2009.
6. Sinha U., *Network Analysis & Synthesis*, 7/e, Satya Prakashan, 2012.
7. Ghosh S., *Network Theory – Analysis & Synthesis,* PHI, 2013.
8. Somanathan Nair B., *Network Analysis and Synthesis*, Elsevier, 2012.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 60% and maximum 80% Problems and Analysis.*

Course outcome:

- At *the end of the course students will be able analyze the electrical circuits and synthesize the electrical circuits.*

13.304 ANALOG COMMUNICATION (T)

Teaching Scheme: 2(L) - 1(T) - 0(P) **Credits**: 3

Course Objectives:

To study the concepts and types modulation schemes. To study different types of radio transmitters and receivers. To study the principles of wired telephone system. Understand the basic principles of digital communication.

Module – I

Amplitude Modulation – Principle of AM, wave forms and analysis, Amplitude modulator circuit, Demodulator circuit. AM Transmitters, Non sinusoidal modulation.

DSBSC Modulation- Principles, Balanced modulator.

SSB modulation-Principles, Advantages. Generation of SSB- Filter method and Phase shift method. Modified SSB systems – Pilot carrier SSB & ISB, Companded SSB.

Module – II

AM Receivers-Super heterodyne receiver, Tuning Range, Tracking, Sensitivity and Gain, Image Rejection, Double Conversion, Adjacent Channel Rejection, Automatic Gain Control.

Noise – Thermal noise, shot noise, partition noise, Flicker noise, Burst noise, Avalanche noise, Bipolar & Field effect transistor noise. Noise factor, Noise factor of amplifiers in Cascade. Noise Temperature. Effect of noise in Analog Communication Systems- Effect of noise on DSBFC AM, Effect of noise on DSBSC AM, Effect of noise on SSB AM.

Module – III

Angle Modulation- Principles of Frequency Modulation, Wave forms and analysis, Comparison between AM and FM.

Phase modulation – Equivalence between PM and FM. Sinusoidal phase modulation. Frequency Modulator Circuits – Basic Reactance modulator, Varactor diode modulator, FM Transmitters – Direct and Indirect methods.

FM detectors - Slope detector, Balanced Slope Detector, Foster Seeley Discriminator, Automatic Frequency Control, Amplitude Limiters, Pre-emphasis and De-emphasis. FM broadcast Receiver.

Effect of noise on Angle Modulation – Threshold effect in Angle Modulation.

Module – IV

Pulse modulation-PAM, PWM, PPM, PCM, companding.

Telephone Systems- Standard Telephone Set. Basic call procedures, Call Progress tones and signals, - DTMF, Cordless Telephones, Electronic Telephones. The telephone circuit- Local

Subscriber loop, Channel noise and noise weighting, Power measurement, Private-line circuits, Voice frequency circuit arrangements, The Public telephone network-Instruments, Trunk circuits and exchanges, Local central office Exchanges, Automated central office switches and Exchanges.

References :

1. Tomasi W., *Electronic Communications System,* Pearson, 5/e,2011.
2. Haykin S., *Communication Systems*, 4/e, Wiley India, 2006.
3. Roody D. and J. Coolen, *Electronic Communication*, 4/e, Pearson, 2011.
4. Proakis J. G. and M. Salehi, *Fundamentals of Communication Systems*, Pearson, 2007.
5. Tomasi W., *Advanced Electronic Communications Systems*, 6/e, PHI, 2012.
6. Kennedy G.*, Electronic Communication Systems*, 4/e, TMH, 2008.
7. Blake R., *Electronic Communication system*, 2/e, Cengage, 2002.
8. Rao P. R., *Analog Communication*, TMH, 2011.
9. Raveendranathan K. C., *Analog Communications Systems,* Universities Press, 2013.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 40% and maximum 60% Problems and Analysis.*

Course Outcome:

At the end of the course the students will be familiar with the modulation schemes and well versed with types of radio receivers. The students will be able to explain the working of wired telephone system and conventional telephone exchange.

13.305 ELECTRONIC CIRCUITS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course Objectives :

- *To study the working of various electronic circuits and their equivalent circuit.*
- *To analyze the different circuits and design the circuits using discrete components as per the specifications.*

Module – I

RC Circuits: Differentiator, Integrator. Diode Circuits: clippers, clampers, multiple diode circuits

DC analysis of BJTs - Transistor Biasing circuits, Load line, BJT as switch, BJT as amplifier. RC Coupled amplifier and its Frequency response. Small signal hybrid π equivalent circuit model. Small signal analysis of CE, CB, CC configurations using Small signal hybrid π model (gain, input and output impedance).

High frequency equivalent circuits of BJTs, Analysis of high frequency response of CE, CB, CC Amplifiers.

Module – II

MOSFET: small signal equivalent circuits. Biasing of MOSFETs amplifiers

Analysis of Single stage discrete MOSFET amplifiers – small signal voltage and current gain, input and output impedance of CS, CG, CD amplifiers, MOSFET Current Source Circuits

MOS differential amplifiers: dc transfer characteristics Small signal equivalent circuit analysis, CMRR, Active load, cascode active load, current mirror circuits.

Module – III

Analysis of Multistage MOSFET amplifiers: Cascade and cascode configuration.

Feedback amplifiers (using BJT): The four basic feedback topologies, Analysis of discrete circuits in each feedback topologies voltage gain, input and output impedance.

Oscillators (using BJT): Barkhausen criterion, Analysis of RC phase shift, Wein Bridge, Hartley, Colpitts, Crystal oscillators. Analysis of BJT tuned amplifiers, synchronous and stagger tuning.

Module – IV

Linear Sweep circuits: Bootstrap sweep and current sweep circuits - analysis.

Power amplifiers: Class A, B, AB and C circuits - efficiency and distortion. Transformer-less power amplifiers.

Power Supply: Rectifiers, Capacitor Filter, Zener diode regulator circuit, design and analysis of series voltage regulator, Short circuit protection. Design of power supply.

References :

1. Sedra A. S. and K. C. Smith, *Microelectronic Circuits*, 6/e, Oxford University Press, 2013 .
2. Neamen D., *Electronic Circuit Analysis and Design*, 3/e, TMH, 2006
3. Spencer R. R. and M. S. Ghausi, *Introduction to Electronic Circuit Design,* Pearson, 2003.
4. Boylestad R. L. and L. Nashelsky, *Electronic Devices and Circuit Theory*, 10/e, Pearson, 2009.
5. Millman J. and C. Halkias, *Integrated Electronics*, 2/e, TMH, 2010.
6. Howe R. and C. Sodini**,** *Microelectronics: An Integrated Approach,* Pearson, 2008.
7. Singh R. and B. P. Singh, *Electronic Devices and Circuits*, 2/e, Pearson, 2013.
8. Gopakumar K., *Design and Analysis of Electronic Circuits*, 2/e, Phasor Books, 2008.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 60% and maximum 80% Analysis, Design and Problems.*

Course Outcome:

At the end of the course, students will be able to analyse the different circuits .Also the students can design circuits using discrete electronic components.

13.306 DIGITAL ELECTRONICS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course Objectives :

- *To study the concepts of number systems.*
- *To study the design of combination logic and sequential logic.*
- *To make the student familiar with internal structure of various digital logic families.*
- *To provide students the fundamentals to the design and analysis of digital circuits*

Module – I

Review of Boolean algebra, Binary arithmetic and Binary codes: BCD, Gray codes, Excess-3 codes, Complement codes.

Logic function representation in Sum of product and product of sum form, Canonical forms, Logic reduction using Karnaugh map and Quine McCluskey method, Introduction to hazards and hazard free design using K-map.

Combinational circuits, Adders, Subtractors, Adder/ Subtractor (4 bit) circuit, ripple carry and look ahead carry adders, BCD adder, decoders, BCD to seven-segment decoder, encoders, key board encoder, multiplexers, de-multiplexers, Function realization using MUX and DEMUX, binary comparators (2/3 bits).

Module – II

Sequential circuits- Latches and flip flops, SR, JK, D, T, race around, edge triggering, Master slave, Excitation table and characteristic equations, state diagram representation, flipflop timing specifications.

Design of binary counters – Synchronous, Asynchronous, Mod-N counters, Random sequence generators, BCD counter, counter IC's (7490, 7492, 7493).

Shift Registers, Shift register counters (Ring and Johnson).

Timing circuits, astable and monostable multivibrators using 555, 74121.

Module – III

Mealy and Moore models, state machine notation, state diagram, state table, transition table, excitation table and equations, state equivalence, state reduction, state assignment techniques.

Analysis and design of synchronous sequential circuits.

Asynchronous sequential circuit – basic structure, equivalence and minimization, minimization of completely specified machines.

Module – IV

Logic families- comparison of logic families in terms of fan-in, fan-out, speed, power, noise margin etc. Basic circuit and working of gates NOT, NAND, AND and OR in CMOS and NAND in TTL logic, interfacing of TTL and CMOS.

Memory devices- Classification, Semiconductor memories, basic circuit and working of static and dynamic RAM, ROM, PROM and EPROM, memory expansion.

Programmable logic devices- PAL, PLA, FPGA, CPLD. Introduction to VHDL- VHDL description for basic gates, flip flops, Full adder, counters (Behavioural model only).

References:

1. Roth (Jr.) C. H., *Fundamentals of Logic Design*, 6/e, Cengage Learning, 2010.
2. Anand Kumar A., *Fundamentals of Digital Circuits*, 2/e, PHI, 2012
3. Yarbrough J. M., *Digital logic- Application and Design,* Thomson Learning, 2006.
4. Wakerly J., *Digital Design Principles and Practice,* 4/e, Pearson, 2012.
5. Floyd T. L., *Digital Fundamentals*, 10/e, Pearson, 2011.
6. Mano M. M. And M. D. Ciletti, *Digital Design*, 4/**e**, Pearson, 2009.
7. DeMessa T. A., Z. Ciecone, *Digital Integrated Circuits*, Wiley India, 2007.
8. Ghoshal S.*, Digital Electronics*, Cengage Learning, 2012.
9. Somanathan Nair B., *Digital Electronics and Logic Design*, 2/e, PHI, 2013.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 50% and maximum 60% Analysis and Design.*

Course Outcome:

The students will be familiar with different digital ICs and be able to design various digital circuits.

13.307 ELECTRONIC DEVICES LAB (AT)

Teaching Scheme: 0(L) - 0(T) - 3(P) **Credits**: 3

Course Objective:

- *The purpose of the course is to enable students to have the practical knowledge of different semiconductor electronic devices.*
- *To study the specifications of devices and circuits.*

List of Experiments:

1. Characteristics of diodes and Zener diode.
2. Characteristics of transistors (CE and CB).
3. Characteristics of JFET.
4. Characteristics of MOSFET.
5. Characteristics of SCR.
6. Characteristics of UJT.
7. RC integrating and differentiating circuits.
8. RC low pass and high pass filters - frequency response characteristics.
9. Zener Regulator with and without emitter follower.
10. RC coupled CE amplifier - frequency response characteristics.
11. MOSFET amplifier (CS) - frequency response characteristics.
12. Clipping and clamping circuits.
13. Rectifiers - half wave, full wave, bridge - with and without filter- ripple factor and regulation

Internal Continuous Assessment *(Maximum Marks-50)*

40% - Test
40% - Class work and Fair Record
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*
Questions based on the list of experiments prescribed.
Circuit and design - 25%,
Performance (Wiring, usage of equipment and trouble shooting) - 15%
Result - 35% ; Viva voce - 25%
Candidate shall submit the certified fair record for endorsement by the external examiner.

Course Outcome:

On successful completion of the course, students will be able to know the working of semiconductor devices and design of circuits using these devices.

13.308 ELECTRONIC CIRCUITS LAB (T)

Teaching Scheme: 0(L) - 0(T) - 3(P) **Credits**: 3

Course Objectives:

- *To study working of electronic circuits.*
- *To design the circuits as per the specifications.*

List of Experiments:

1. Feedback amplifiers (current series, voltage series) - gain and frequency response.
2. Power amplifiers (transformer less) - Class B and Class AB.
3. Differential amplifier using MOSFET - Measurement of CMRR.
4. Cascade amplifier using MOSFETs – gain and frequency response.
5. Cascode amplifier using MOSFETs - frequency response.
6. Oscillators – RC phase shift, Wien bridge, Hartley and Colpitt's.
7. Tuned amplifier - frequency response.
8. Series voltage regulator.
9. Bootstrap sweep circuit.
10. Introduction to SPICE and simulation of experiments 4, 5, and 6 listed above using SPICE

Internal Continuous Assessment *(Maximum Marks-50)*

40% - Test
40% - Class work and Fair Record
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours Maximum Total Marks: 100

Questions based on the experiments No.1 to 9 in the above list.

Circuit and design - 25%,

Performance (Wiring, usage of equipment and trouble shooting) - 15%

Result - 35% ; Viva voce - 25%

Candidate shall submit the certified fair record for endorsement by the external examiner.

Course Outcome:

After successful completion of the practical student will be able to analyse and design electronic circuits.